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Nanoelectromechanical contact switches

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Nanoelectromechanical (NEM) switches are similar to conventional semiconductor switches in that they can be used as relays, transistors, logic devices and sensors. However, the operating principles of NEM switches and semiconductor switches are fundamentally different. These differences give NEM switches an advantage over semiconductor switches in some applications — for example, NEM switches perform much better in extreme environments — but semiconductor switches benefit from a much superior manufacturing infrastructure. Here we review the potential of NEM-switch technologies to complement or selectively replace conventional complementary metal-oxide semiconductor technology, and identify the challenges involved in the large-scale manufacture of a representative set of NEM-based devices.

The success of the semiconductor industry is based, in part, on scalable manufacturing processes and reliable performance. However, as semiconductor devices become smaller and applications become increasingly demanding, alternative and complementary approaches will be needed. Nanoelectromechanical (NEM) switch technologies are being investigated because they offer reduced leakage currents[1–3] — which leads to reduced power consumption and improved ON/OFF ratios[4,5]. The power consumed by conventional semiconductor devices (that is, by CMOS — complementary metal-oxide semiconductor — devices) increases as they are scaled to smaller sizes, so the reduced power consumption offered by NEM devices — and also by hybrid NEM–CMOS devices[6] — is highly advantageous. Modelling predicts that NEM switches will have READ and WRITE times in the sub-nanosecond range, but this has not been demonstrated yet[4,7,8].

Nanoelectromechanical technology is also relatively insensitive to radiation[9], temperature[10] and external electric fields[8], which makes it well suited for the harsh environments encountered in aerospace and defence applications. Moreover, logic gates built from NEM switches require fewer components than comparable gates built from CMOS components[11–13]. NEM-switch architectures are unlikely to replace CMOS, but they are being explored as components in various transistor, memory, logic and sensing applications, as is evidenced by patent applications[14–18] and research papers[4,9,11,12,19–31] (Fig. 1).

In this Review we examine the future of NEM-switch technologies through a representative set of devices (Table 1) and identify two primary roadblocks[1,2]: a lack of methods for scalable manufacturing and poor device reliability. We then discuss the developments needed in materials, engineering, manufacturing and fundamental science to overcome these roadblocks. We focus on electrostatically actuated NEM switches in which there is intermittent mechanical contact between an active element and an electrode. We do not cover research into the use of NEM resonators[32–35] for applications such as the ultrasensitive detection of mass, force and displacement[36,37], high-frequency signal processing[38], and ultrahigh-frequency oscillators[39]. However, the manufacturing challenges facing both these branches of NEM technology are very similar.

Basic operating principles and power consumption

Nanoelectromechanical switches work by using electrostatic forces to mechanically deflect an active element into physical contact with an opposing electrode, thus changing the state of the device. The electrostatic forces scale inversely with the square of the gap between the active element and the electrode[40], making them increasingly effective as devices get smaller. As the voltage applied across the active element and the electrode is increased, the resulting electrostatic forces are balanced by elastic restoring forces in the active element. When a critical 'pull-in' voltage is reached, the electrostatic forces overwhelm the restoring force: this causes the active element to accelerate towards the electrode, which closes the switch and leads to a sharp rise in the current through the device (which is usually much sharper than the rise seen in CMOS devices). This pull-in voltage depends on the device geometry and can be predicted by a variety of analytical and computational methods (Box 1).

After the switch has closed, elastic restoring forces in the deformed active element act to pull the switch open. Adhesive forces at the contact between the active element and electrode counteract this, holding the switch closed. If the elastic restoring forces are insufficient to break the adhesion when the electrical bias is fully removed, the switch will behave in a non-volatile manner, remaining in the closed state even when no input is applied (Fig. 2a). However, if the switch is designed such that the elastic forces of the deformed active element are sufficient to overcome the adhesive forces, the switch will be volatile and re-open when the applied bias is sufficiently reduced (Fig. 2b).

In general, stiffer active elements and larger gaps between the active element and the electrode favour volatile operation as they lead to greater elastic restoring forces in the deformed active element when the switch is closed[27,41]. However, this comes at the expense of higher actuation voltages and a greater propensity for electrothermal failure modes. In contrast, more compliant active elements and smaller gaps favour non-volatile operation and lower actuation voltages. In either case, the balance of forces results in a current–voltage response that exhibits a characteristic hysteretic loop that can be exploited to achieve bistability, which is a basic requirement for various memory and logic devices (Fig. 2a,b).

Different electrode architectures can be used to produce different functionalities. In two-terminal devices, for example, a single opposing electrode is used both as a drain and as a gate to pull the active element into contact (Fig. 2c). Three-terminal NEM switches are generally designed such that a gate electrode can push or pull the active element into contact with the drain electrode[10,11,20,29,42–44], controlling the current through the device in a manner similar to a conventional transistor (Fig. 2d,e and

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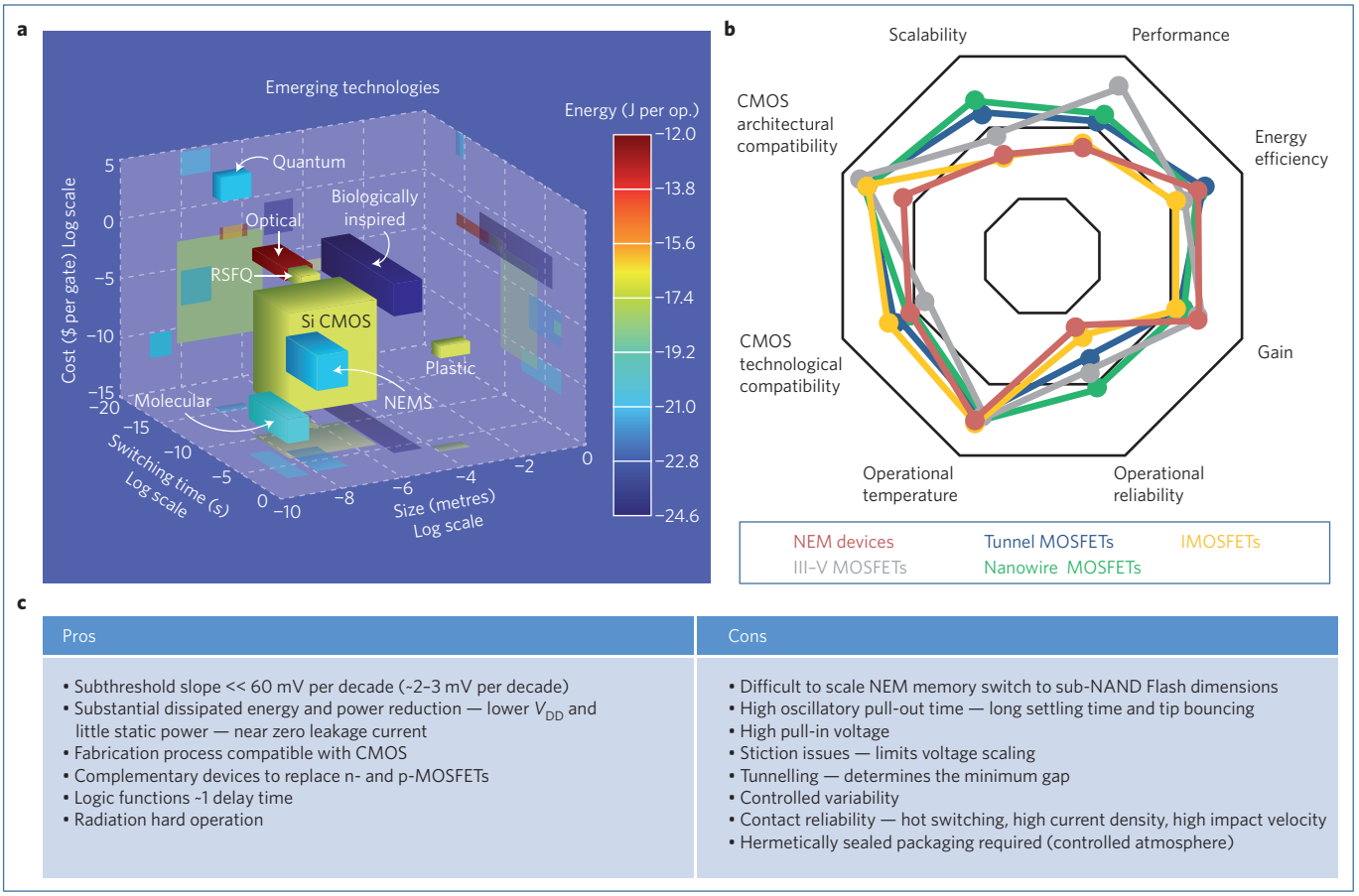


Figure 1 | Comparing the performance of NEM technology with CMOS and other emerging technologies. a, The 2005 edition of the International Technology Roadmap for Semiconductors[114] (ITRS) compared the performance of CMOS and seven emerging technologies in terms of cost, switching time and size (all on log scales). The energy per operation (J per op.) is represented by colour. Nanoelectromechanical switches compete well in terms of energy per operation, but suffer from relatively long switching times. However, it is important to note that NEM and many other emerging technologies are being developed to complement rather than replace CMOS. RSFQ: rapid single flux quantum. **b**, The 2009 edition of the ITRS[1] compared NEM devices with several types of MOSFETs (metal–oxide–semiconductor field-effect transistors) in terms of eight parameters including performance and energy efficiency. Relative performance improves with distance along the radial axis. Although NEM switches compete well in terms of energy efficiency, CMOS compatibility and operational temperature, their reliability and scalability need to be improved. **c**, The pros and cons of NEM-switch-based memory as identified in the report from the 2010 ITRS Future Memory Devices Workshop[2]. Panels reproduced with permission from: **a**, ref. 114, © 2005 ITRS SEMATECH; **b**, ref. 1, © 2009 ITRS SEMATECH.

Table 1). Additional functionality can be achieved by using more complex electrode architectures (Fig. 2f), or connecting two or more NEM switches to make a logic gate. For example, two NEM switches can be used to make a four-terminal XOR gate, whereas it would take at least ten CMOS transistors to make such a gate[12].

In conventional CMOS transistors, subthreshold leakage (that is, the small current that is present in the OFF state) has increased substantially as the critical dimensions scale down[4]. More recently, however, gate leakage has started to overtake subthreshold leakage, and together these parasitic losses will soon consume more than half of the total input power.

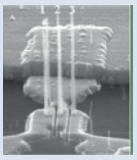
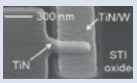
In contrast, the physical gap between the source and drain terminals in an open NEM switch means that the subthreshold leakage is limited to vacuum tunnelling and Brownian motion displacement currents. These leakage currents are often quantified in terms of the subthreshold swing, which should be as low as possible: the minimum possible subthreshold swing for a CMOS device is ~60 mV per decade at room temperature, and much lower swings (below 3 mV per decade) have been reported for NEM devices[5,19]. In three-terminal NEM devices with independent gate and drain electrodes (Fig. 2d,e), gate leakage remains largely unaffected when the switch is closed and remains limited by tunnelling and Brownian motion[4]. Thanks to their ability to limit leakage, hybrid NEM–CMOS systems are being pursued as a way to maintain or improve CMOS performance while continuing to be scaled down (Box 2).

Despite the reduced leakage currents, power consumption is a concern for NEM switches because it scales with the operating frequency and the square of the voltage. As a result, NEM switches often consume less total power than the equivalent CMOS systems at low frequencies, but they become less efficient than CMOS above a certain frequency. This transition occurs at ~150 million operations per second for 32-bit adders[11]. The fact that it generally takes fewer NEM switches than CMOS transistors to make a logic circuit helps to offset this problem to some degree. Moreover, the reduced leakage current in hybrid NEM–CMOS devices allows the use of smaller components elsewhere in the circuit, which in turn reduces dynamic switching power: for example, a reduction of 60% has been reported for hybrid OR gates[4].

Progress so far

The International Technology Roadmap for Semiconductors (ITRS)[1,2] identifies emerging technologies with the potential to sustain Moore's law. These technologies include CMOS-based approaches, such as multi-level and multi-gate devices, and entirely

Table 1 | Representative NEM-switch architectures.

	Device	Structure (no. of electrodes)	Primary materials	Fabrication methods	WRITE 1 (0) voltage (V)	ON/OFF ratio	R_{ON}* (kΩ)	Cycles (~order)	Failure modes	Notes	Year	Ref.
1		Crossbar single NS (3)	CNT ropes	Manipulation	2.5 (40)	10	10^2	1	—	5 x 5 nm unit size	2000	23
2		Cantilevered single NS (2/3)	Carbon nanofibre/ nanotube, Au	EBL, DEP	3	10^5	10	1	Burn-out, stiction	100 μA current	2003–2006	30, 42, 47, 53, 58
3		Suspended ensemble (2)	CNT, Pd	CNT film, EBL	5 (6)	10^4	10^2–10^3	10^7	—	—	2004–2007	9, 22, 52
4		Suspended single NS (3)	CNT, Au	Dispersion, EBL	3.5	10^4	10^4	1	—	—	2005	45
5		Vertical single NS (3)	CNT	EBL, NS growth	24 (25)	10^4	10^3	1	Burn-out, stiction	—	2005	20, 29
6		Suspended single NS (2)	CNT, Nb	NS growth, EBL	2.5	10^4	10–10^4	1	—	2.8 ns switch time	2006	59
7		Telescoping single NS (2)	CNT	EBL, DEP	0.8 (2)	—	10^2–10^3	1	Burn-out, stiction	220 nm pitch	2006–2010	61, 93, 108
8		Cantilevered ensemble (3)	CNT (bulk)	NS growth, EBL	50	10^7	10^3	10	Stiction	100 μA current	2008	43
9		Cantilevered thin film (3)	TiN	EBL, CMOS, ALD	12	10^5	< 10^6	10^3	Wear, burn-out, stiction	CMOS fabrication <3 mV per decade	2008	19, 48
10		In-plane cantilevered thin film (3)	SiC	EBL	6	—	—	10^9	Fracture, melting	500 °C temperature	2010	10

Ten NEM-switch architectures listed in chronological order. The following information is given for each architecture: general device structure and number of electrodes; primary materials used; fabrication methods used; WRITE (ERASE) voltages; ON/OFF current ratio, resistance of switch in ON state (approximate order), number of cycles without failure (approximate order); failure modes. *Unless stated explicitly in the reference, the ON resistance is estimated from reported current–voltage plots; in cases where an upper bound is stated, the current was limited by the compliance of the characterization equipment. CNT: carbon nanotube; NS: nanostructure; EBL: electron-beam lithography; ALD: atomic layer deposition; DEP: dielectrophoresis. Scale bar in row 8, 2 μm.
Images reproduced with permission from: **row 1**, ref. 23, © 2000 AAAS; **row 2**, ref. 42, © 2005 IOP; **row 3**, ref. 52, © 2004 IEEE; **row 4**, ref. 45, © 2005 AIP; **row 5**, ref. 20, © 2005 AIP; **row 6**, ref. 59, © 2006 ACS; **row 7**, ref. 93, © 2007 IOP; **row 8**, ref. 43, © 2008 NPG; **row 9**, ref. 48, © 2008 AIP; **row 10**, ref. 10, © 2010 AAAS.

new approaches such as molecular devices and NEM switches. Researchers have already reported using NEM switches in electrical switches[19,20,27,28,45–51], relays[8,21,30], memory elements[9,22,23,27,28,52], logic devices[13,21,25,53] and sensors[36,54]. However, NEM technology is more likely to be used to complement CMOS (as in hybrid devices) rather than to compete with it.

Table 1 contains a representative set of NEM switches that we will use to discuss the potential of NEM-switch technologies, and also the challenges associated with using these technologies in real-world applications.

Nanotube-based crossbar memory. These devices consist of two layers of transverse nanotube ropes separated by a nanometre-scale gap. Data is stored in the non-volatile two-terminal switches created where the nanotube ropes cross and make contact when actuated. An analysis of the competing energies (elastic, van der Waals and electrostatic) yielded design envelopes in which the device would behave in a bistable manner. Actuation (WRITE) voltages of ~2.5 V for these devices are comparable to the voltages used in conventional dynamic random access memory technology[23].

Box 1 | Analytical description of NEM device operation.

Nanoelectromechanical contact switches are broadly categorized by the boundary conditions on the active element: a cantilever is fixed at one end, whereas a suspended beam is fixed at both ends. Based on these boundary conditions, classical beam analysis can be used to approximate the response of the active element to applied electrostatic forces. Although van der Waals interactions between the active element and contact electrode are often neglected for microelectromechanical systems, they must be considered for NEM switches[41].

Here we consider the simpler case of a cantilever and use beam theory to derive the following equation for the balance of the elastic force (left of the equation) against the van der Waals force q_{vdw} and the electrostatic force q_{elec} (per unit length)[51]

$$EI\frac{d^2}{dx^2}\left(\frac{\frac{d^2w}{dx^2}}{\left(1+\left(\frac{dw}{dx}\right)^2\right)^{3/2}}\right)\frac{1}{\sqrt{1+\left(\frac{dw}{dx}\right)^2}}=(q_{vdw}+q_{elec})$$

where E is the Young modulus, I is the second moment of area, x is the position along the cantilever ($x = 0$ at the fixed end), and w is the transverse displacement at x.

The van der Waals force is generally described using a Lennard–Jones potential[51], and the electrostatic force scales with the square of the applied voltage. To model real devices it is necessary to include variations in the distributions of charge and electrostatic force along the active element, and also nonlinear deformation[12,27,51,73]. The pull-in voltage V_{PI} can then be determined by performing an instability analysis on this equation (see below).

To model the dynamic behaviour of the device it is necessary to also include the acceleration and damping of the active cantilever element

$$\rho A\frac{\partial^2 r}{\partial t^2}+c\frac{\partial r}{\partial t}+EI\frac{\partial^4 r}{\partial x^4}=q_{elec}+q_{vdw}$$

where $r(x,t)$ is the gap between the nanotube and electrode at position x and time t, ρ and A are the density and cross-sectional area of the active element, respectively, c is a damping constant depending on the quality factor, and it is assumed that the displacements are small ($dw/dx<<1$ in the beam equation above). Unlike in the quasi-static case, q_{elec} now depends on the time-varying bias charge on the active element, which in turn is largely dependent on the resistances and capacitances of the system (and is not necessarily equivalent to the externally applied voltage V)[27]. This equation can be used to estimate device response times and the dynamic stresses encountered by the active element[27]. (This equation can also be adapted for a suspended beam: see ref. 51 for details.)

Type of device	Pull-in voltage[51]
Cantilever	$V_{PI}\approx k_s\sqrt{1+K_S^{FK}}\,\frac{H}{L^2}\ln\left(\frac{2H}{R_{ext}}\right)\sqrt{\frac{EI}{\varepsilon_0}}$
	$k_s\approx 0.85,\ K_S^{FK}\approx\frac{8H^2}{9L^2}$
Suspended	$V_{PI}=k_D\sqrt{1+K_D^{FK}}\,\frac{H+R}{L^2}\ln\left(\frac{2(H+R)}{R}\right)\sqrt{\frac{EI}{\varepsilon_0}}$
	$k_D=\sqrt{\frac{1{,}024}{5\pi S'(c_{PI})}\left(\frac{c_{PI}}{H+R}\right)}$
	$K_D^{FK}=\frac{128}{3{,}003}\left(\frac{c_{PI}}{\rho}\right)^2,\quad \rho^2=\frac{I}{A}=\frac{R_{ext}^2+R_{int}^2}{4}$
	$S(c)=\sum_{i=1}^{\infty}\left(\frac{1}{\left[\ln\left(\frac{2(H+R)}{R}\right)\right]^i}\sum_{j=1}^{\infty}a_{ij}\left(\frac{c}{H+R}\right)^j\right)$

L: length of the active element; H: gap between the undeflected active element and electrode; R_{ext} and R_{int}: external and internal radius of the active element, respectively; $R=R_{ext}$; ε_0: permittivity of vacuum; c_{PI}: central deflection of the active element at pull-in; a_{ij}: known constants[51].

Cantilevered nanostructure switches. These devices consist of an individual nanostructure cantilevered over a metallic electrode. In general, the nanostructures have a high Young modulus (1 TPa for carbon nanotubes[55]), resulting in high natural frequencies and allowing faster response. Multiwalled nanotubes or doped nanowires are often used because they are known to be conductors; single-walled nanotubes, on the other hand, are usually avoided because only one third of single-walled nanotube structures are metallic — the other two thirds are semiconducting. (This mixture of metallic and semiconducting behaviour is also a problem when trying to fabricate field-effect transistors (FETs) based on individual single-walled nanotubes[56,57].) Both two-[49–51] and three-terminal[58] architectures have been demonstrated. In general, strong hysteretic behaviour in the current–voltage response was observed[26,27,53], with the experimentally measured pull-in voltages[47] matching theoretical predictions. Sub-5-V actuation voltages were also reported[30,42]. Moreover, sharp switching behaviour was observed with ON/OFF current ratios[47] on the order of 10^5 and ON currents on the order of 100 μA (ref. 30). By replacing the commonly used metal thin-film electrodes with diamond-like carbon structures, it was shown that the lifetime of these devices can be significantly extended[27,53].

Suspended nanostructure switches. An individual nanostructure is fixed at both ends and suspended over an electrode, and they have been constructed in two-[46,59] and three-terminal[42,45] configurations. Because they are fixed at both ends, these devices are stiffer, allowing faster mechanical response times than cantilevered devices of comparable dimensions, albeit at higher actuation voltages, although sub-5-V actuation has been reported[46,59], along with sub-3-ns switching times[59].

Cantilevered nanostructure ensembles. These devices consist of cantilevered structures cut from dense mats or fabrics of carbon nanotubes[43]. These three-terminal switches exhibit ON/OFF ratios of 10^7. Although larger than the single-nanostructure devices, the

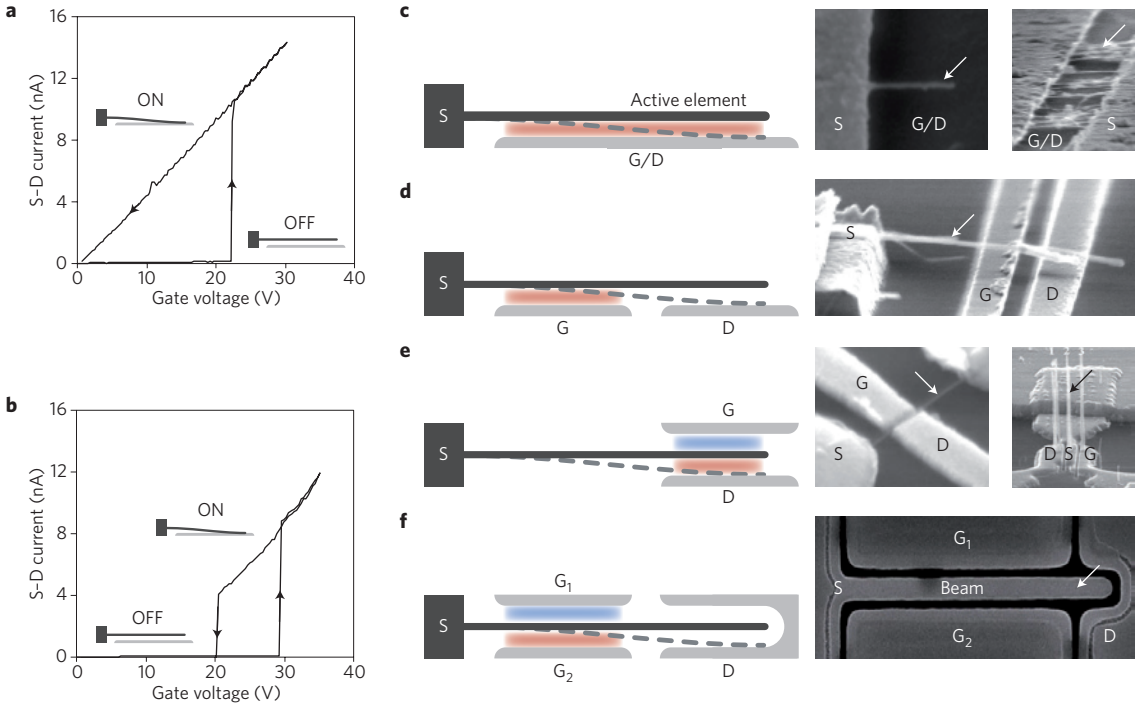


Figure 2 | Basic operating characteristics of NEM switches. a,**b**, Current versus voltage for NEM devices exhibiting non-volatile (**a**) and volatile (**b**) behaviour[27]. As the voltage is increased the current remains zero until the pull-in voltage is reached and the active element makes contact with the electrode (inset). The current then increases linearly with the voltage. However, when the voltage is reduced below the pull-in voltage, adhesive forces between the active element and electrode hold them together and the current either decreases linearly with the voltage (**a**) or drops back to zero at a lower voltage when the stiffness of the active element overcomes the adhesive force (**b**). The fact that there can be two stable states for a given input voltage (between pull-out and pull-in) can be exploited in memory applications. **c**–**f**, Schematics (left) and micrographs of various NEM devices showing the source (S), drain (D), gate (G) and active element (white arrow). In general, the active elements in these devices range from a few hundred nanometres to a few micrometres in length. Red and blue indicate attractive and repulsive electrostatic forces in the schematics. **c**, Two-terminal architecture in which a voltage is applied to the source electrode and a single gate/drain electrode, producing an electrostatic force that pulls the active element into contact with the gate/drain electrode. **d**, A three-terminal architecture in which a voltage is applied to the source and gate electrodes, producing an electrostatic force that pulls the active element into contact with the drain electrode. **e**, A three-terminal architecture in which the electrostatic force pushes the active element into contact with the drain electrode. Note that the drain and gate electrodes can also be individual nanostructures[20] rather than conventional planar electrodes as shown here. **f**, The possibility of making more complex architectures, such as this device with two gate electrodes, means that logic gates built from NEM switches require fewer components than comparable gates built from CMOS components. The active elements in these schematics are all cantilevered structures: however, active elements can also be suspended at both ends and deflect in the plane of the substrate or out of this plane. Panels reproduced with permission from: **a**,**b**, ref. 27, © 2011 Wiley; **c**, (left) ref. 53, © 2012 Wiley, (right) ref. 52, © 2004 IEEE; **d**, ref. 42, © 2005 IOP; **e**, (left) ref. 45, © 2005 AIP, (right) ref. 20, © 2005 AIP; **f**, ref. 12, © 2010 ACM.

use of mats or fabrics carries several advantages: as the entire mat is electrically conductive, a single lithography step can, in principle, be used to define the active element, the electrodes and other electrical circuitry traces from the same material layer. To demonstrate this, arrays of thousands of these switches were fabricated on a single substrate starting from a dense layer of carbon nanotubes[43].

Suspended nanostructure ensembles. In these devices, the active elements are fabricated from dense mats[9,22,52] or other ensembles of single-walled nanotubes, rather than an individual one-dimensional nanostructure. This brings manufacturing advantages (see below), and also avoids the semiconducting-versus-metallic problem for single-walled nanotubes, and devices capable of millions of non-volatile switching cycles, with READ/WRITE voltages below 5 V and sub-10-ns READ/WRITE times, have been demonstrated[22]. Progress reports from this technology have slowed recently though, suggesting that challenges in scalable manufacturing remain[60].

Vertical nanostructures. This variation of the cantilevered single-nanostructure switches uses vertically oriented nanotubes as the active element and also as the gate and drain electrodes[20]. This design, which was developed jointly by Samsung and several academic institutions, facilitates greater integration densities than in-plane architectures, and has been used to demonstrate extremely stable, non-volatile READ/WRITE operations[29].

Telescoping nanostructures. These two-terminal devices are made by creating a break in a suspended multiwalled nanotube: this switch can be closed by applying an electrical bias to bring the two separated halves of the nanotube back into contact with each other. Like the crossbar nanotube memory, the individual elements of these devices are extremely small, enabling multiple switches to be constructed on a single nanotube, and opening up the possibility of ultrahigh integration densities. Furthermore, relatively low sub-1-V actuation voltages have been demonstrated[61].

Cantilevered thin-film devices. These devices consist of active elements cut from thin films using various lithography and etch processes in a top-down manner. The gap between the thin-film active element and underlying electrode is generally defined using

Box 2 | Hybrid NEM–CMOS devices.

The properties of two hybrid NEM–CMOS devices — dynamic OR gates and SRAMs — are summarized in the table below. Individual hybrid NEM–CMOS devices can also be combined to create more complex systems. For example, individual SRAM cells (either hybrid or purely NEM-based) can be combined with CMOS decoders to form look-up tables or SRAM-based field-programmable arrays[3]. There have also been proposals to build hybrid SRAM devices in which carbon nanotubes are used as the active elements of the NEM switches and also as the channel of the transistors[116]. The challenges associated with integrating NEM switches and CMOS are discussed in Box 3.

Type of device	Result
Dynamic OR gate In this device three three-terminal NEM switches are placed in series below a conventional NMOS (n-type metal-oxide semiconductor) pull-down network[4].	Significantly lower subthreshold leakage of the NEM switches reduces leakage in the pull-down network because they are in series. Lower leakage in pull-down networks also enables use of a smaller keeper, which in turn reduces switching power by 60–80%.
Static random access memory This device can be made by replacing two of the pull-down transistors in a conventional six-transistor CMOS–SRAM cell with three-terminal NEM switches[44].	Static power dissipation reduced by 85%. Improvement in hold (> 2) and read (> 3) static noise margins Allows maintained cell stability with continued scaling (difficult to maintain stability while scaling conventional six-transistor CMOS–SRAM cells). Decreased READ and WRITE delays dependent on ON resistance of the NEM switches (delays do not depend on mechanical switch delay). Note, an exception to the decreased delay is when a WRITE is followed immediately by a READ. In this case, the NEM switch must be conducting before the READ can be executed, and thus is limited by the mechanical delay.

a sacrificial film that is selectively etched away to release the device. This is a key advantage of this approach because the thickness of the sacrificial film can be defined down to ångström resolution using techniques such as atomic layer deposition. This approach (along with the in-plane devices described below) is perhaps the most scalable of the approaches we discuss because it has its roots in the microelectromechanical systems (MEMS) industry, which shares many manufacturing techniques with the semiconducting industry. For example, cantilevered devices fabricated from thin films of titanium nitride using conventional CMOS processing have demonstrated ON/OFF ratios of 10^5 and sub-threshold slopes below 3 mV per decade[19], and CMOS-compatible tungsten switches have achieved ~50,000 successful actuation cycles before the eventual mechanical failure of the beam[62]. These advantages may also facilitate more straightforward manufacturing of hybrid NEM-switch–CMOS devices[4].

In-plane cantilevered thin-film devices. These devices are similar to those described in the previous section, but they deflect in the plane of the substrate. A key advantage is the ability to define complex, multi-terminal device architectures in a single lithography and etch process. In contrast, defining a device that deflects perpendicular to the substrate (with electrodes above and below the active element) would be challenging using present manufacturing techniques. Three-terminal in-plane switches in which the active element and the electrodes were micromachined from silicon carbide thin films operated for billions of cycles at temperatures as high as 500 °C, which is well above the temperature at which conventional CMOS devices degrade[10]. Other silicon carbide switches have achieved pull-in voltages as low as 1 V and metallizing these switches enabled sub-10 kΩ ON resistances to be demonstrated[63]. The complexity of the electrode configurations that can be defined with this approach means that it is possible to make an adder based on NEM switches that contains fewer than half the total number of transistors needed for CMOS-based adders[11].

The challenges of scaling

The devices described in Table 1 were primarily one-off laboratory-scale demonstrations, rather than large-scale arrays of devices. Moreover, there was often a significant gap between the performance predicted by modelling or simulation[31,41] and the actual performance. In many cases, this gap was due to limitations in current manufacturing techniques that constrain experimental devices to non-optimal geometry or materials. Another common trait was the use of inherently serial processes — such as the use of nanomanipulators to position individual nanostructures[23,26,27,47] or the need for electron-beam lithography to define metallic contacts to randomly oriented nanostructures[45,64] (Fig. 3a) — that are not amenable to wafer-scale production. (These concerns also apply to many other device architectures, such as solid-state devices made from graphene[65], nanotubes[56] or nanowires[66,67], and NEM resonators[34,35].)

Given that the semiconductor industry continues to improve the performance of a variety of lithography, deposition and etching techniques, the outstanding obstacle to scaling the manufacture of NEM switches is the lack of techniques that can control the position of nanostructures in large numbers. For laboratory-scale experiments, small numbers of nanostructures are often randomly dispersed on the substrate, which means that standardized masks or reticles cannot subsequently be used to define the electrical contacts. If it were possible to control the positions of the individual nanostructures, scalable tools from the semiconductor industry could rapidly replace the laborious serial processes used at present. Below we discuss a number of techniques that might make this possible.

Creating arrays of nanostructures on device substrates. Low-dimensional nanostructures can be grown directly on the device substrate for subsequent device fabrication. For example, nanotubes can be grown by chemical vapour deposition (CVD) from catalysts such as iron[68] or cobalt[69] nanoparticles, ferritin protein[70] and thin metal films[20,71,72], with the nanotube diameter depending on the size of the catalyst particles[68]. The pull-in voltage is sensitive to the stiffness of the active element[41,51,73] (Box 1), so

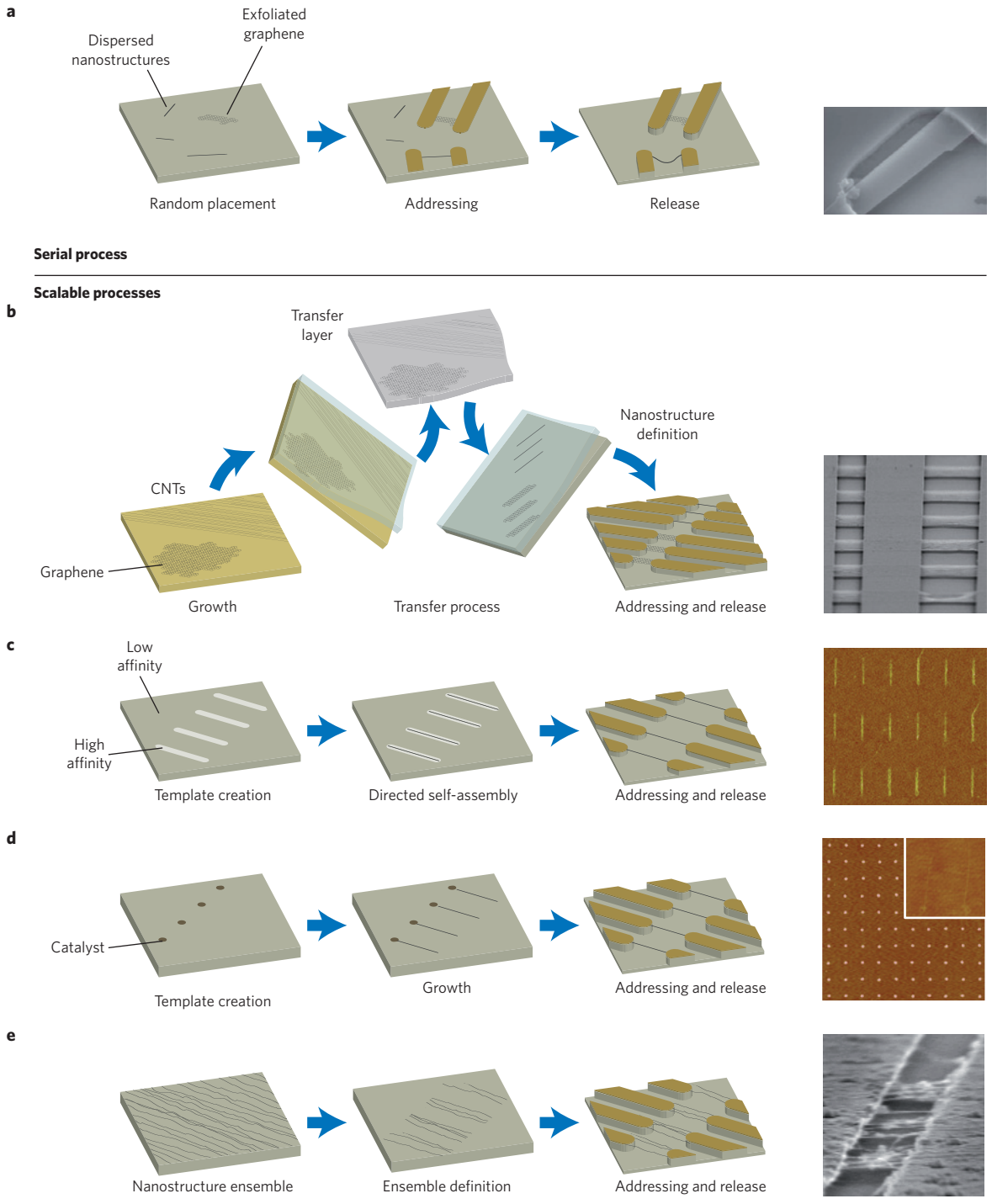


Figure 3 | Different approaches to manufacturing processes for NEM switches. Schematics showing some of the different methods used to make NEM switches and micrographs (far right) showing actual devices. **a**, The most commonly used method to construct NEM switches involves the random placement of nanostructures (left) followed by customized addressing and release. **b**, Another approach is to grow the nanostructure on a substrate that is optimized for growth, and then transfer it to a substrate that is optimized for devices. The nanostructures can be patterned by etching prior to transfer or after transfer. Here, graphene is grown on a copper foil, transferred to a silicon oxide substrate, and patterned with lithography and etch techniques to make resonators[115]. **c**, Directed self-assembly involves creating a template with regions of greater and lesser affinity for a given material. The template is then placed in a solution containing this material and nanostructures assemble in the regions of greater affinity. **d**, In patterned growth methods, CVD is used to grow nanostructures from catalysts placed at particular positions on the growth substrate. **e**, Nanostructure ensembles, such as dense mats of carbon nanotubes, can be grown or deposited on the substrate, and then patterned and addressed. These ensembles can also be transferred to another substrate as in **b**. Panels reproduced with permission from: **a**, ref. 64, © 2007 AAAS; **b**, ref. 115, © 2010 ACS; **c**, ref. 89, © 2006 PNAS; **d**, ref. 87, © 2009 Northwestern Univ.; **e**, ref. 52, © 2004 IEEE.

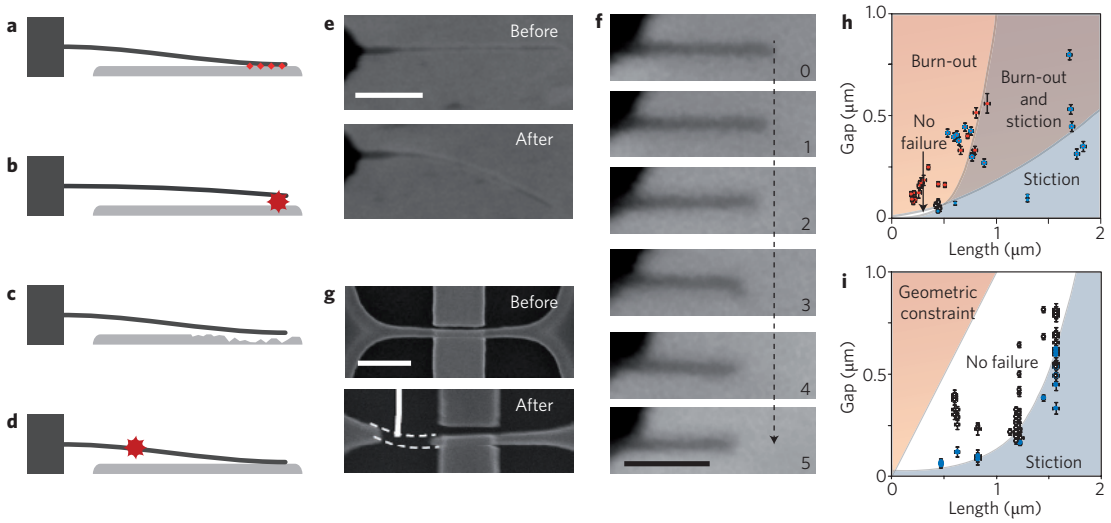


Figure 4 | Common failure modes for NEM switches. a–g, Schematics and scanning electron micrographs of common failure modes for NEM switches. **a**, Irreversible stiction between the active element and electrode. **e**, A nanotube-based NEM switch before and after suffering from irreversible stiction[27]. **b**, Damage to the active element and/or electrode caused by electrical discharge on pull-in. **f**, Series of micrographs captured following successive actuation cycles of a NEM switch, showing the length of the nanotube decreasing monotonically due to electrical-discharge-induced ablation of the tip[27]. **c**, Electrode damage due to wear, exacerbated by electrical discharge. **d**, Mechanical fracture or fatigue of the active element. **g**, Micrographs of a NEM switch before and after failure by fatigue/fracture[111]. **h**,**i**, Maps of failure modes for two-terminal nanotube-based NEM switches using a gold (**h**) or diamond-like carbon (**i**) electrode[27]. The *x*-axis is the length of the active element (the nanotube); the *y*-axis is the size of the gap between the active element and the electrode at rest. The use of diamond-like carbon significantly increases the region of parameter space in which no failure occurs. Scale bars are 500 nm (**e**,**f**,) and 300 nm (**g**). Zero electrical bias is applied in both images in **e**. Panels reproduced with permission from: **e**,**h**,**i**, ref. 27, © 2011 Wiley; **g**, ref. 111, © 2009 IEEE.

being able to control the diameter in this way can help achieve uniformity in device performance. Laminar gas flows and applied electric fields can also be used to control the orientation of the nanostructures as they grow. Certain substrates, notably quartz[74] and sapphire[75], provide even higher levels of control over the orientation because nanostructure growth occurs along specific crystallographic orientations but, unfortunately, these substrates are often not suitable for integrated device fabrication: for example, hybrid NEM–CMOS devices require silicon substrates. Similarly, highly uniform graphene growth is achieved on substrates that are not amenable for device fabrication, such as copper[76]. However, a number of processes have been developed to transfer these nanostructures onto more suitable substrates after growth (see 'Transfer processes' below).

By patterning the catalyst prior to growth (Fig. 3d), the placement of nanotubes on the device substrate can also be controlled[20,54,69,74,77–80]. Various tools can be used to pattern the catalyst arrays. In microcontact printing for example, a polymer relief stamp is used to transfer catalyst 'ink' to the substrate, allowing large regions to be patterned with a single pressing. The resolution is generally limited to the micrometre scale, though some variations of this approach allow resolution down to single particles[80].

In dip-pen nanolithography[81], scanning probes are dipped in catalyst ink that diffuses onto the substrate as the probe is moved across it, allowing dot arrays of catalyst with feature sizes of ~500 nm up to micrometres to be made[79]. It is also possible to combine the advantages of the microcontact and dip-pen approaches by using stamps that consist of arrays of soft polymer probes[82] or hard probes with a soft polymer backing[83] to produce uniform, high-resolution, high-density patterning over large areas. However, catalyst patterning has not yet been demonstrated with this combined approach.

Nanofountain probes[84–86] are also based on scanning probes and rely on the delivery of a continuous supply of ink from on-chip reservoirs to a tip, thus removing the need for repeated re-inking of the tips. This approach has been used to create large-scale arrays of nanotube catalyst with sub-100-nm resolution (Fig. 3d)[87]. Electron-beam lithography[70,88] can also be used to pattern catalysts.

In directed self-assembly, templates consisting of regions of greater and lesser affinity for the nanostructures are created on a substrate. Nanostructures in liquid suspension are then selectively captured in regions of greater affinity to create the desired pattern[89]. This approach has been used to construct two-terminal cantilevered and suspended multiwalled nanotube devices[46] on pre-defined gate/drain electrodes (Fig. 2c). Although the observed yield was lower than that when using single-walled nanotubes[89,90], the selectivity of the assembly was high, which is an advantage for scaling up to large arrays.

The techniques used to pattern catalysts can also be used to create the templates for directed self-assembly (Fig. 3c). For example, dip-pen nanolithography has been used to define thiol-based templates on gold substrates on which well-ordered arrays of single-walled nanotubes were assembled[89,90]. Lithography[88] and microcontact printing[91,92] have also been used to create the templates for directed self-assembly.

Dielectrophoresis — the use of non-uniform electric fields to apply forces to particles (which do not need to be charged) — has also been used to selectively capture nanotubes[61,93,94] and nanowires[95] at electrode sites for subsequent device fabrication (row 7 in Table 1). When a liquid suspension of nanostructures is placed in a field between adjacent electrodes, an effective dipole moment (and thus a torque) is produced due to their polarizability, causing the nanostructures to align with the field[96]. Dielectrophoresis has been used to separate semiconducting and metallic nanotubes, based on the difference in their dielectric constants[96,97], and is highly efficient in assembling large numbers of nanotubes, but is less well suited to aligning single nanotubes because they don't align precisely or form bundles[30,98,99]. However, techniques have been developed to turn off the applied electric field once the first nanotube has bridged electrodes[100]. Another challenge lies in incorporating the electrodes used for dielectrophoresis into the device.

Transfer processes. Because many of the techniques described in the previous section work best on substrates that are not well suited to device manufacturing, a number of processes have been developed to transfer nanostructure arrays to substrates that are more suitable for device fabrication[74,101,102]. After the nanostructures have been produced on an optimized substrate (Fig. 3b), a soft handle layer is deposited over the nanostructures. The initial substrate is then etched away[76], or the handle layer is peeled away. The handle layer — which contains the nanostructures — is then transferred to the device substrate. The nanostructures can be patterned before or after the transfer[103]. In other cases, growth substrates were designed such that they could be inverted to transfer grid-like networks of nanotubes directly to the device substrate without the need for a handle layer[78].

Ensembles of nanostructures. So far we have focused on the fabrication of devices containing individual low-dimensional nanostructures because these are likely to lead to the greatest gains in performance in the long term. However, working with ensembles of nanostructures is, perhaps, an intermediate and more readily attainable solution. For example, dense mats of single-walled nanotubes can be cut to produce active elements that behave like a monolithic thin-film beam[9,22,43,52] (Fig. 3e). Similar techniques have been used to create nanotube-based FETs with excellent mobility and ON/OFF ratios for ring oscillators and various flip-flop circuits[104]. Though generally larger than single-nanostructure devices, these active elements have the advantage that they can be defined by lithography and etching processes similar to those used to make devices based on thin films, which is good for scalability. Moreover, these ensembles are good electrical conductors because their charge-transport properties are dominated by metallic nanotubes, which leads to reduced power consumption. NASA has tested nanotube-based memory devices developed by Lockheed Martin and Nantero on the space shuttle[105].

Thin-film devices. A variety of vertically and laterally actuated cantilever and suspended beam NEM switches have been fabricated in a top-down manner by alternately depositing and then patterning or etching thin films using processes borrowed directly from the established semiconductor and MEMS industries. For example, titanium nitride cantilevered NEM switches (row 9 in Table 1) with cantilever–electrode gaps as small as 15 nm were fabricated using conventional CMOS processes[19,48]. The reduced fabrication challenges associated with thin-film devices have also enabled greater flexibility in pursuing alternative electrode configurations for logic applications[11]. Ultimately, fabricating NEM switches with CMOS-compatible processes (either thin-film devices or by adapting the low-dimensional nanostructure fabrication methods) will facilitate rapid scaling, integration, and as discussed, realization of hybrid NEM–CMOS devices.

Going forward. Scaling up the manufacturing of NEM switches will require advances in patterning, wafer-scale nanostructure growth and transfer techniques. However, once methods have been developed to create well-ordered arrays of nanostructures, it will be possible to take advantage of existing fabrication techniques such as high-resolution lithography and thin-film technology.

Materials selection also has a profound impact on device performance. For example, contact resistance is dictated by the combination of active element and electrode material used. A higher contact resistance helps to mitigate failure by electrical discharge[27,53], but it also increases electrical delay[31,44] and power consumption, and decreases stability. A nanotube–gold contact typically has a contact resistance ~1 kΩ, whereas a nanotube–diamond-like-carbon contact typically has a much higher resistance (~1 GΩ) (ref. 27). The optimization of contact resistance will be crucial to the development of devices based on NEM switches, and although some of the lessons learned en route to the large-scale manufacture of highly reliable microscale switches will be relevant, it will be necessary to take into account the changes in material properties that occur at the nanoscale.

The Young modulus of the active element is also important: a high value will lead to a high natural frequency (and hence a faster response), but it will also lead to higher pull-in voltages. The Young modulus for commonly used materials ranges from hundreds of gigapascals (for silicon[106] and silicon carbide[107]) to ~1 TPa for carbon nanotubes[55]. The hardness and wear resistance of both the active element and the electrode material will also become increasingly important for long-term performance and reliability[19,48].

Ultimately, one-dimensional nanostructures are expected to offer the best performance, but they also present greater challenges in terms of manufacturing and the tuning of device properties, so thin-film devices are more likely to feature in real-world applications in the short and medium term.

Device reliability

In addition to scaling up manufacturing and meeting predicted performance levels, we must address the challenge of increasing device reliability by reducing common failure modes, such as wear and tear, and damage caused by electrical discharges. By examining the representative set of NEM switches in Table 1, we see that these failure modes become more common as devices reduce in size from thin films through nanostructure ensembles to individual one-dimensional nanostructures.

As mentioned above, adhesive forces between the active element and the electrode keep the switch closed as the electrical bias is reduced, and in some cases the switch will remain closed even after the bias has been completely removed. This phenomenon, known as stiction, is exacerbated if localized heating welds the active element and the electrode together. As with contact resistance, advances in the MEMS industry may serve as a guide to tackling stiction in nanoscale switches: however, it will also be necessary to allow for differences in the relative magnitudes of van der Waals and elastic forces, and in the significance of surface roughness relative to the dimensions of the active elements.

For volatile NEM switches, irreversible stiction is considered a mode of failure (Fig. 4a). On larger scales, cantilevers cut from dense ensembles of nanotubes stuck in the closed position irreversibly after 23 successive cycles[43]. Two- and three-terminal NEM switches constructed from individual nanotubes also suffered similar irreversible stiction (Fig. 4e)[30,47,108]. However, researchers have shown that coating a suspended nanotube in a two-terminal switch with a layer of atoms can reduce adhesion[46], enabling tens of cycles of reversible switching, although the benefit is found to reduce with further cycling, probably due to damage caused by high electrical currents. The use of alternative electrode materials can also reduce adhesion. For example, nanotube NEM switches that have diamond-like carbon electrodes suffer less adhesion than switches with gold electrodes[27]. The diamond-like carbon therefore gives much greater flexibility in the geometric design of devices (Fig. 4h,i).

In the case of non-volatile devices, stiction is desirable as it does not require continued power input to hold the switch in the closed state. To break the stiction and reverse the state of the switch, a voltage pulse is often applied to the active element and one of the electrodes[20,22,23]. This voltage is often much higher than the pull-in voltage: 40 V is needed to break the adhesion of the crossbar device shown in Table 1 (row 1), compared with a pull-in voltage of less than 5 V (ref. 19). Improvements in both materials and design (especially of the contact region) are needed to reduce this voltage.

Ablation or localized melting of the active element and/or contact electrode (also known as burn-out) can also cause problems (Fig. 4b,c). When the switch is open, the active element forms a capacitor relative to the opposing contact electrode. As the applied bias is ramped up,

Box 3 | The challenges of integrating NEM switches and CMOS.

The three primary requirements of NEM switches for hybrid devices are: to maintain low pull-in voltages; to provide robust and consistent performance over many actuation cycles; and to be small enough to perform at a high level while also being large enough to be reasonably fabricated[41]. In many cases, these requirements place conflicting demands on the design of devices. For example, more compliant beams reduce pull-in voltages but are prone to irreversible stiction. However, as fabrication methods improve and alternative materials are introduced, the restrictions on the design of devices will be relaxed (Fig. 4h,i). This table summarizes some of the challenges associated with integrating NEM switches and CMOS.

Challenge	Current status and conflicting goals
Matching required NEM switch pull-in voltages with current CMOS operating levels (often <1 V)[44].	Some devices have achieved sub-5-V actuation (see Table 1), others require upwards of 50 V. Devices with sub-5-V actuation often still require significantly larger pulses to break adhesion and re-open the switch due to the relatively high compliance of their active elements. Achieving volatile operation with sub-1-V actuation is especially difficult, as more compliant devices favour irreversible (non-volatile) stiction due to decreased elastic restoring forces.
Operation in air (or required encapsulation)[44].	The majority of NEM switches demonstrated so far were operated in vacuum. Rate of switch deterioration degrades rapidly in air with successive actuation cycles due to increased opportunity for: oxidation, capillary adhesive forces, other surface contaminants that can dramatically affect interaction between the active element and contact electrode. The need for encapsulation increases space requirements and adds manufacturing complexity.
Increasing ON currents and decreasing ON resistance[4].	So far, devices report ON resistances (dominated by contact resistance R_c between the active element and contact electrode) ranging from kΩ to GΩ. Lower R_c improves static noise margin[44] but increases susceptibility to burn-out on pull-in[27]. Larger R_c has the opposite effect. ON currents as high as 100 μA have been reported, though nA levels are more common. For a given input voltage $>V_{PI}$, the ON current is strongly tied to R_c.
Scaling devices and contacts[31].	Elastic restoring force on a NEM-switch cantilever decreases more quickly than either van der Waals or capillary forces that act to cause stiction[117]. Properties of contact between active element and commonly used metal electrodes (R_c, stiction, wear) deteriorates rapidly with scaling[117]. Alternatives to commonly used metal thin-film electrodes (for example, doped diamond-like carbon[27,53] or thin coatings[48]) may allow tailored contact properties and expand available design space.
Actuation times[2]	At present, reported actuation times are in the nanosecond range or higher, whereas CMOS operate well into the gigahertz range. Stiffer devices have higher natural frequencies, but require higher actuation voltages. Pull-out time may be significantly longer than pull-in time, with long settling periods and tip bouncing. In some cases, systems can be designed such that longer delay/actuation times do not affect overall device speed. For example, hybrid NEM–CMOS SRAM cells were designed such that the relatively slow NEM switches did not limit overall circuit speed[44].

charges build in this capacitor as well as other parasitic capacitances. When the switch closes, these stored charges dissipate rapidly through the active element, resulting in an initial spike in current that can be orders of magnitude greater than the steady-state ON current. For the relatively low contact resistances common to metal electrodes, simulations predict that the resulting discharge current densities can be sufficient to ablate the active element or damage the electrode[27].

Examples of burn-out are widespread. Nanoscale titanium nitride beams were completely destroyed on closing[48]. Cantilevered switches constructed from individual carbon nanofibres[30,42] or multiwalled nanotubes[20,27,47] suffered from partial loss of the tip of the nanostructure active element with repeated cycling (Fig. 4f). Telescoping multiwalled nanotube devices experienced similar ablation of the nanotube shells[61], resulting in rapid degradation of switching characteristics.

Perhaps the most straightforward way to reduce burn-out is to decrease the gap between the active element and electrode, or to reduce the stiffness of the active element, thus reducing the required actuation voltage and amount of energy stored in the system. However, this comes at the expense of favouring the stiction failure mode and thus places limits on the device geometries that are possible for a given choice of materials[27].

The rate of discharge (and thus the resulting current density when the switch closes) is largely determined by the RC time constant, where R is the contact resistance and C the capacitance between the active element and the electrode. Intuitively, increasing

this resistance should slow the rate of discharge and thus reduce the current density towards the steady-state value. For example, the addition of ultrathin oxide coatings can increase the effective contact resistance in the thin-film titanium devices described previously: it has been shown that such a device can be operated for several hundred cycles before the switching characteristics began to deteriorate as the oxide coating wears away[19,48] (Fig. 4c). The use of insulating liquid media to surround the switch — as opposed to air or vacuum — has also been shown to improve switch lifetime (by reducing arcing) and to decrease the pull-in voltage[109].

The contact resistance between a nanotube and doped diamond-like carbon is significantly higher than that between a nanotube and an electrode made of gold or some other metal, so the use of doped diamond-like carbon eliminates ablation of the nanotube by reducing the rate of charge dissipation when the active element makes contact with the electrode[27]. This significantly increases the size of the no-failure region available to device designers (Fig. 4h,i), and has allowed cantilevered NEM switches to survive more than one million actuation cycles[53]. There are, however, disadvantages associated with high contact resistances: increased power dissipation and delays[31,44], and decreased static noise margin[110]. Thus, as in the case of beam compliance, it will be necessary to find a balance between the advantages associated with a high contact resistance (such as reduced ablation) and the disadvantages (such as increased power consumption). Research is also needed to find new materials that will, like diamond-like carbon, make it easier to manufacture devices by increasing the size of the no-failure region.

Whereas fatigue and fracture in general have been found to be less prevalent in micro- and nanoscale devices, the apparent fracture of active elements has been observed in some NEM switches (Fig. 4d,g)[10,62,111]. For example, silicon carbide cantilevered NEM switches have failed as a result of fracture, or a combination of fracture and melting when operated at high temperatures, after one billion operating cycles[10]. Suspended silicon beam structures have also failed by apparent fracture after fewer cycles[28,111]. In general, however, the mechanical stresses experienced by the nanostructures are generally significantly less than their fracture strength[27], so in the absence of defects, they should only experience elastic strain (for example, stretching of the C–C bonds in a nanotube) rather than fracture.

Outlook

Through the past decade, the outstanding performance achieved in small numbers of NEM switches has earned these devices a place in the ITRS roadmap as potential successors or hybrid complements to conventional CMOS[1,2]. Although the next decade will see a continued focus on demonstrating new types of functionality in NEM-based devices, greater emphasis will be placed on scaling and integration. Important challenges include improving reliability and developing methods that are able to create well-ordered arrays of nanostructures. It is encouraging to note that many of the other challenges associated with the manufacture of NEM-based devices have already been conquered by the current semiconductor industry.

As it is not possible to construct large-scale arrays of NEM switches at present, it is also not possible to perform the parametric studies that are needed to fully optimize device designs (for example, to identify the best geometries and materials to balance the competing effects of mechanical compliance, contact resistance and so on) in a statistically significant manner. Analytical and computational models that can predict the highly dynamic and inherently multi-physics response of devices (in which the electrical, mechanical and thermal responses are all coupled to each other) will therefore become increasingly important. And as devices continue to scale down, these models will need to include quantum effects such as the Casimir effect (which can, for example, influence the gap at which pull-in occurs[112,113]). Modelling is also needed to improve the yield from various nanomanufacturing techniques[89].

The first applications of NEM-based switches are likely to be in niche areas, such as ultralow power or high-temperature systems, where scalability and speed are less critical. The introduction of fully integrated electromechanical computing architectures will involve overcoming the challenges associated with NEM–CMOS integration, such as matching operating voltages and packaging concerns (Fig. 1c and Box 3). As manufacturing methods and device architectures continue to evolve, NEM-switch performance will begin to approach that predicted in models. Once this has been achieved, NEM–static-random-access-memory (SRAM) architectures and other hybrid systems may rival conventional CMOS devices in terms of switching speeds while offering reduced power consumption[4]. Finally, as NEM switches are pushed to compete more directly with CMOS transistors in performance, the adoption of the single-nanostructure architectures will potentially facilitate the highest levels of performance, although this will also involve overcoming enormous scientific and technological challenges.

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Additional information

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