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Thermoelectric voltage at a nanometer-scale heated tip point contact

Patrick C Fletcher, Byeonghee Lee and William P King

Department of Mechanical Science and Engineering, University of Illinois at Urbana-Champaign, Urbana, IL, USA

E-mail: wpk@illinois.edu

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Abstract

We report thermoelectric voltage measurements between the platinum-coated tip of a heated atomic force microscope (AFM) cantilever and a gold-coated substrate. The cantilevers have an integrated heater–thermometer element made from doped single crystal silicon, and a platinum tip. The voltage can be measured at the tip, independent from the cantilever heating. We used the thermocouple junction between the platinum tip and the gold substrate to measure thermoelectric voltage during heating. Experiments used either sample-side or tip-side heating, over the temperature range 25–275 °C. The tip–substrate contact is ∼4 nm in diameter and its average measured Seebeck coefficient is 3.4 μV K^{-1}. The thermoelectric voltage is used to determine tip–substrate interface temperature when the substrate is either glass or quartz. When the non-dimensional cantilever heater temperature is 1, the tip–substrate interface temperature is 0.593 on glass and 0.125 on quartz. Thermal contact resistance between the tip and the substrate heavily influences the tip–substrate interface temperature. Measurements agree well with modeling when the tip–substrate interface contact resistance is 10^8 K W^{-1}.

(Some figures may appear in colour only in the online journal)

1. Introduction

Heat transfer at point contacts has been an area of intense research [1–8]. In scanning thermal microscopy (SThM) [6, 7, 9–12], a scanning probe tip with an integrated temperature sensor measures highly localized temperature or thermal conductivity. The point contact heat transfer governs the accuracy of these measurements. There has been significant interest in the development of atomic force microscope (AFM) cantilevers with integrated heaters [13–20], which can apply a controlled, nanometer-scale heat source to a substrate. Such a nanometer-scale hot spot has applications for characterizing [21–27] or modifying [28–30] thermally sensitive samples at the nanometer scale. An understanding of the tip–substrate interface temperature is critical for the further development and application of these technologies.

The interface temperature between a nanometer-scale tip and substrate has been historically difficult to establish due to challenges in understanding thermal conduction through the substrate, the tip–substrate contact area, and the quality of the interfacial contact between tip and substrate [5–7]. Published research has investigated the heat flow processes and tip–substrate interface temperature for heated silicon AFM cantilevers with experiments [5] and modeling [4, 31]. One approach to calibrate the interface temperature is to observe the tip interaction with polymer substrates having a known glass transition [32] or heat-induced crystallization [24] temperature. However, these results depend on tip geometry and require that the tip–substrate thermal conductance does not change after calibration.

Temperature sensing with SThM probes is usually performed by measuring the thermoelectric voltage of a thermocouple positioned near the tip–substrate interface. The thermocouple junction is either near the tip [6, 7] or at the interface [1–3]. The tip temperature is calculated from the measured thermoelectric voltage and a calibrated Seebeck coefficient [7, 9, 10]. In previous work, the goal has been to measure the junction temperature that results from sample-side heating. Sadat *et al* used a point contact thermocouple scheme to map interface temperature fields with sample-side heating and demonstrated ∼10 mK temperature resolution and <100 nm spatial resolution [3]. A more

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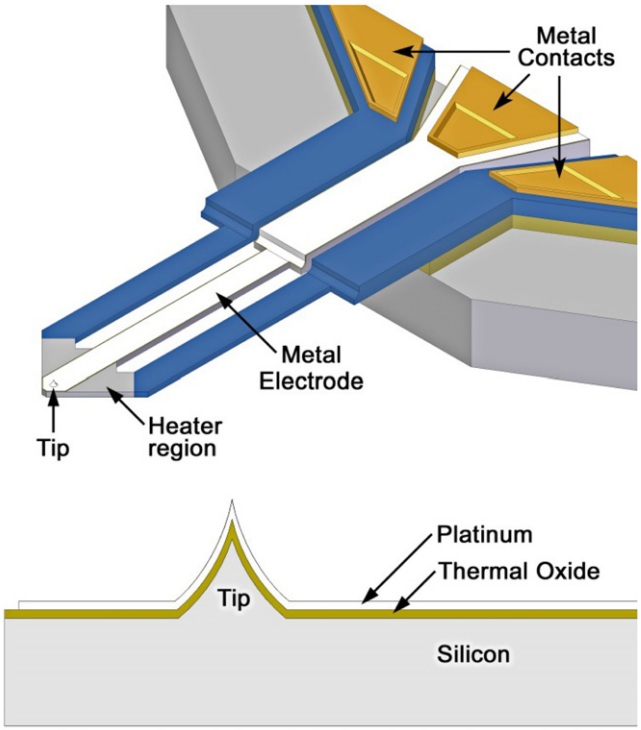

Figure 1. Schematic diagram of an electro-thermal (ET) microcantilever with integrated solid-state heater. Two cantilever legs, high-doped N+ type, address a resistive heater, low-doped N type, while the third platinum-coated leg addresses the cantilever tip at the end of the cantilever. The heater region and tip electrode are electrically isolated with a thin layer of silicon dioxide.

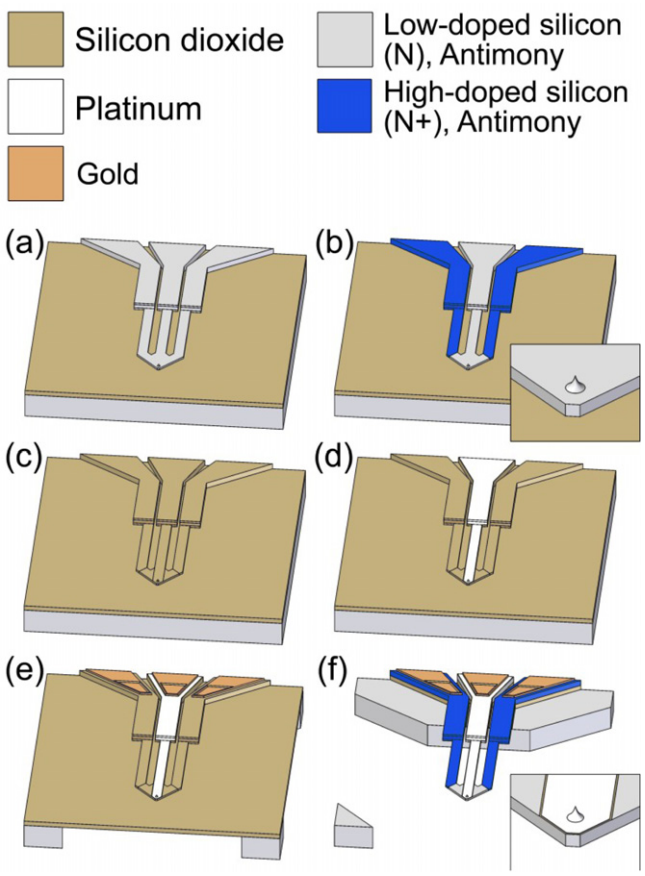

Figure 2. Summary of fabrication steps. (a) Fabrication begins with an antimony-doped silicon-on-insulator (SOI) wafer. First, we form the cantilever anchor regions and a dull tip using an ICP-DRIE, then sharpen the silicon tip using an oxidation sharpening technique. Another ICP-DRIE to the oxide box layer defines the final cantilever beam shape. (b) Next, we dope the high-doped N+ type regions using ion implantation of antimony and subsequently (c) grow a thin thermal oxide in an oxidation furnace. (d) The metal tip electrode is formed through sputter deposition and lift-off of platinum. (e) We fabricate electrical contacts by coating the cantilever with a silicon dioxide insulating layer, exposing vias to the high-doped silicon, and depositing gold traces. The device handle is created with backside ICP-DRIE through 500 μm of silicon, using the buried oxide layer as an etch stop. (f) Finally, the sacrificial oxide layers are dissolved in hydrofluoric acid, releasing the ET cantilever.

complete understanding of the tip–sample thermal transport could be enabled by comparing this type of measurement with tip-side heating.

This paper presents measurements of thermoelectric voltage at the thermocouple point contact junction when the temperature rise is a result of tip-side heating. The experiments used an electro-thermal (ET) cantilever [33] in contact with metal-coated substrates to form a point contact thermocouple. We determined tip–substrate interface temperature from the calibrated thermoelectric voltage.

2. Cantilever design and fabrication

The ET cantilever combines the functions of a cantilever having an integrated heater and a cantilever having a metal probe tip. Figure 1 shows the design of the metallized ET cantilever. The device has three legs of length 155 μm, width 20 μm, and thickness 1 μm. The legs extend from thicker anchor beams whose presence allows the cantilever spring constant to be tailored, since the cantilever spring constant is dictated by the length of the cantilever legs protruding from the anchor beams, rather than where the device chip edge intersects the cantilever legs using a less precise fabrication process. Two of the legs are connected in series to a resistive heater region and the third leg is used to address the conductive scanning probe tip. We fabricate the heater using low-doped silicon because of its ability to self-heat to high temperatures [32] and suitability for batch fabrication [13]. The heater region dimensions were selected such that the heater electrical resistance would be close to 2.2 kΩ [14]. The tip electrode is a 40 nm thick platinum (Pt) trace, which forms a conductive pathway along a third cantilever leg to the probe tip. The heater and tip electrode are separated with a 25 nm thick thermally grown silicon dioxide, which electrically isolates the tip from the heater until the voltage difference between tip and heater exceeds the voltage breakdown of the oxide.

Figure 2 shows the ET cantilever fabrication steps. We fabricate the metallized ET microcantilevers on a 100 mm silicon-on-insulator (SOI) wafer with a handle layer thickness of 500 μm, a silicon dioxide buried oxide (BOX) layer thickness of 1 μm, and a device layer thickness of 5 ± 0.5 μm

with resistivity 0.01–0.05 Ω cm doped N type with antimony. First, we etch to form the cantilever anchor regions and the dull tips using an inductively coupled plasma (ICP) deep reactive ion etch (DRIE) 2 μm into the silicon device layer, then use an oxidation sharpening technique [34] to sharpen the silicon tips to about 10 nm in radius. An ICP-DRIE through the remaining silicon device layer to the oxide BOX layer defines the final cantilever beam shape. Next, we deposit and pattern a 300 nm plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide mask and dope the high-doped N+ type regions using ion implantation of antimony with an acceleration energy of 120 keV and a concentration of 2×10^{16} cm^{-2}. Following the first ion implantation, we remove the mask oxide and deposit a diffusion barrier PECVD oxide 300 nm thick, then anneal the dopant in N_2 at 1000 °C for 60 min and 1100 °C for 150 min. A wet etch removes the barrier oxide, then we grow 25 nm of thermal oxide in an oxidation furnace at 950 °C. After the oxide growth, we pattern a photoresist mask for the metal tip electrode and deposit a 10 nm sputtered chromium adhesion layer beneath 40 nm of sputtered platinum. The unnecessary metal and photoresist are removed through lift-off in acetone. The excess thermal oxide will be removed later in a self-aligning process where only the oxide beneath the Pt trace will remain. A layer of PECVD oxide 300 nm thick protects the tip and electrode during subsequent fabrication. We open vias in the PECVD oxide down to the high-doped silicon microcantilever legs and fabricate electrical contacts with a 10 nm sputtered chromium adhesion layer beneath 250 nm of sputtered gold. The cantilever devices are further protected with 400 nm of PECVD oxide and we etch through the SOI handle layer from the backside to the sacrificial silicon dioxide layer with an ICP-DRIE etch. Finally, the cantilevers are released by removing the BOX layer, protective PECVD oxide, and thermal oxide in concentrated hydrofluoric acid (HF) for 20 s.

Figure 3 shows a fabricated ET cantilever. The characterization and calibration of similar probes has been reported elsewhere [33]. The key feature of this cantilever is that the tip can be heated to a controlled temperature in a manner that is independent from the measured voltage at the tip. The tip has an average radius of 50 nm and is conformally coated with a 25 nm oxide and 40 nm of sputtered Pt. The average cantilever resonant frequency is 42.7 ± 2.5 kHz, the quality factor is 45.0 ± 3.6, and the spring constant is 0.57 ± 0.12 N m^{-1}; these mechanical properties were measured in an Asylum MFP-3D AFM system. The device yield was ∼75%, with a 100 mm SOI wafer producing ∼400 cantilevers. The primary mode for fabrication failure is undercutting of the thermal oxide by the concentrated HF during release, which allows the metal tip electrode to electrically short with the resistive heater region.

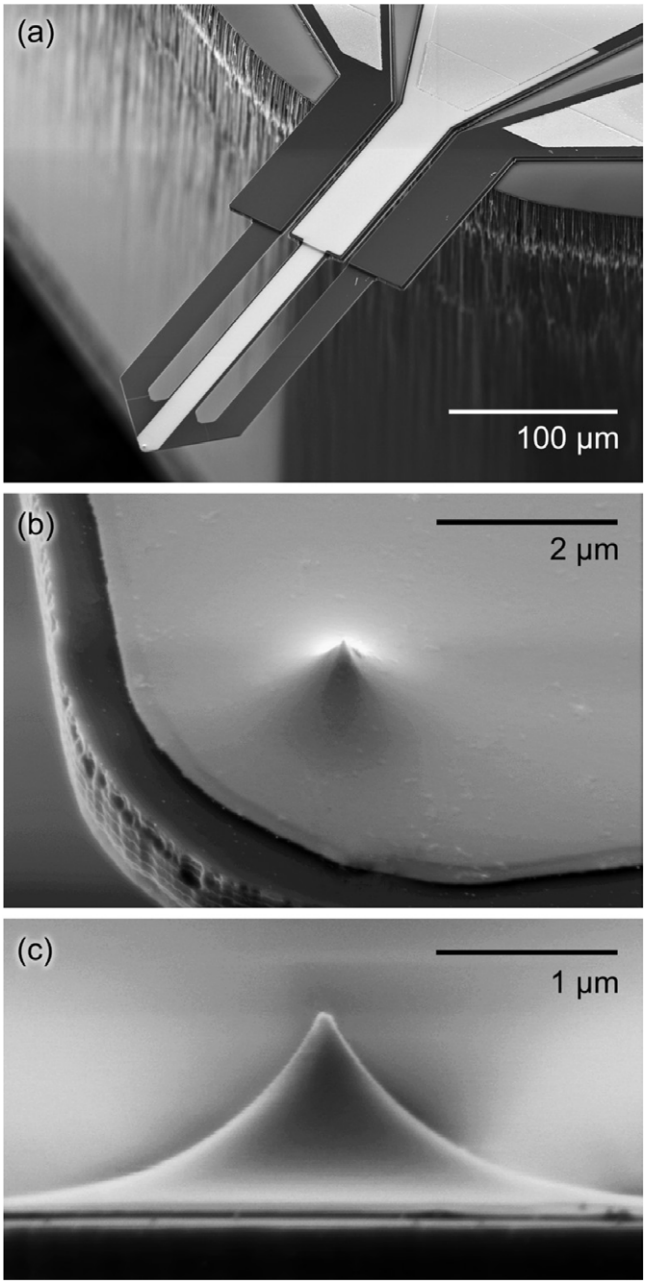

Figure 3. SEM micrographs of a fabricated silicon cantilever with integrated solid-state heater and platinum electrode. (a) The outer cantilever legs control a resistive heater, while the center leg is an electrical pathway to the cantilever tip. (b) The platinum-coated tip is located at the apex of the microcantilever. (c) The tips have an average radius of 50 nm across the wafer.

3. Experiment

In order to form a thermocouple junction between the tip and substrate, the substrates were sputter coated with 100 nm of gold (Au). We chose Pt for the tip electrode and Au for the substrate electrode because they have a large difference in bulk Seebeck coefficients: +2.86 μV K^{-1} for Au versus −7.9 μV K^{-1} for Pt. The substrate was either soda-lime glass or quartz, which have thermal conductivities of 1.1 and 9.4 W m^{-1} K^{-1}, respectively.

Figure 4(a) shows the experiment circuit diagram for measuring thermoelectric voltage using an ET cantilever with Pt electrode contacting a Au-coated substrate. The ET cantilever was mounted in an Asylum Research MFP-3D AFM such that there was independent electrical connection to each of the three active cantilever legs. The substrate was fixed on a temperature-controlled stage and the

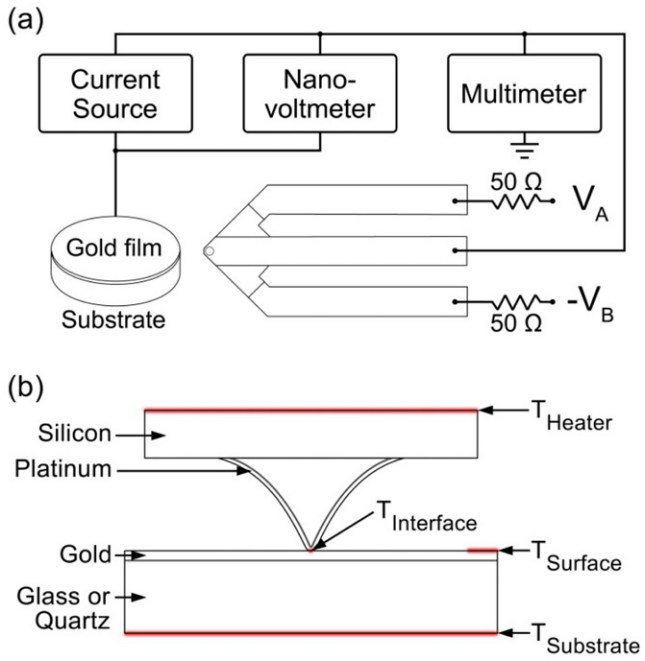

Figure 4. Experimental setup. (a) Experimental setup where the voltage across the heater, $V_A - (-V_B)$, was balanced such that the tip electrode was 0 V. (b) Diagram of a heated tip in contact with a substrate showing relevant temperatures, not to scale.

experiment was conducted in air at 20 °C. Figure 4(b) shows the tip–substrate system and the relevant temperatures, which are the cantilever heater temperature, T_{Heater}, the tip–substrate interface temperature, $T_{Interface}$, the substrate surface temperature away from the tip, $T_{Surface}$, and the substrate temperature, $T_{Substrate}$.

First, we measured point contact thermoelectric voltage, V_{TC}, with substrate temperature, $T_{Substrate}$, varied over the range 30–100 °C without cantilever heating. The cantilever was brought into contact with the substrate with a load of 10 nN. The Pt-coated tip and Au-coated substrate formed a point contact thermocouple generating thermoelectric voltage, V_{TC}, which was measured by a nanovoltmeter five times for each temperature. The temperature was selected in random order to avoid hysteresis effects. During substrate heating we did not monitor T_{Heater}, which was certainly above room temperature from heat conduction through air. However, V_{TC} depends only on $T_{Interface}$ [3].

Second, V_{TC} was measured as a function of cantilever heater temperature, T_{Heater}, without substrate heating. Cantilever heater temperature was calibrated and controlled using known methods [13, 32]. The relationship between cantilever heater resistance and temperature was calibrated using Raman spectroscopy, a non-contact spectroscopic technique that measures temperature based on the Stokes peak position shift. We focused a 488 nm Ar+ laser through a 50× objective to a focal spot 1 μm in diameter on the cantilever heater, near the tip. To avoid laser heating, the laser power was reduced to 45 μW. Spectra were gathered over 60 s intervals such that the peak height was at least 2000 photoelectron counts. The experiments were performed with the same procedures as used for the substrate heating

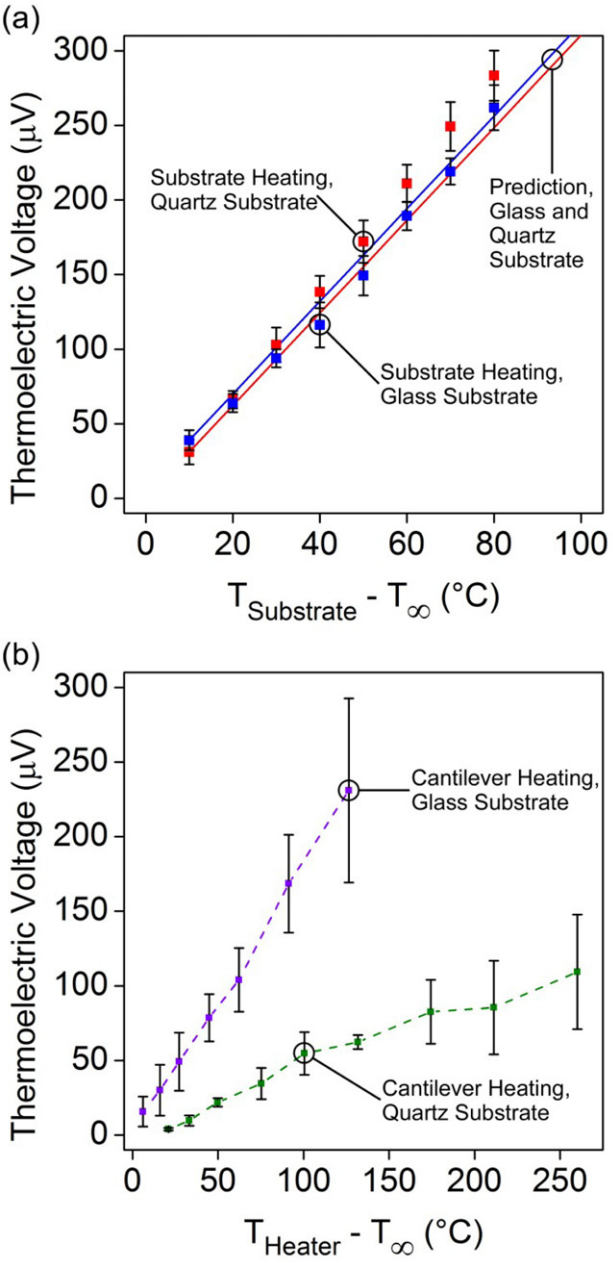

Figure 5. Measured thermoelectric voltage at the tip–substrate interface for (a) substrate heating and (b) cantilever heating. The substrate was either soda-lime glass or quartz. The temperature of the ambient environment is T_∞. For substrate heating, the average measured Seebeck coefficient is 3.4 μV K^{-1}.

experiments. The cantilever was heated while the tip was retracted from the surface and the input voltages V_A and $-V_B$ were balanced until the voltage potential at the tip electrode was 0 V, after which the tip was brought into contact with the substrate.

4. Results and discussion

Figure 5 shows the measured thermoelectric voltage for either substrate or cantilever heating. For sample-side heating, the slope of a linear fit to the experimental data is 3.16 μV K^{-1}

for glass and 3.62 μV K^{-1} for quartz. These values agree well with each other, which is expected since the thermocouple type is the same in each case. These values also agree with the published value of 3.10 μV K^{-1} for a Pt–Au thin film thermocouple with a platinum thickness of 40 nm [8, 35]. Substrate heating represents a nearly isothermal condition throughout the sample, including the tip–substrate interface region. This is expected since the thermal resistance between the substrate and Au film is very small compared to the resistance between the substrate and the surrounding air. The average measured V_{TC} as a function of $T_{Substrate}$ yields a Seebeck coefficient of 3.4 μV K^{-1}. For cantilever heating, the thermoelectric voltages on glass and quartz substrates differ significantly. The thermoelectric voltage V_{TC} is lower on the quartz substrate than on the glass substrate for a given T_{Heater}. This can be explained by the thermal conductivities of the underlying substrates, which differ by an order of magnitude. The standard deviation of V_{TC} for cantilever heating increases with temperature, which is seen in other published results [3]. The increase in variability of V_{TC} with temperature may be the result of Johnson–Nyquist thermal noise, which is electronic noise that increases with increasing temperature.

We calculate tip–substrate interface temperature from the measured thermoelectric voltage using the Seebeck coefficient, measured during sample-side heating. The cantilever heating experiment yields V_{TC} as a function of T_{Heater}, and likewise the substrate heating experiment yields V_{TC} as a function of $T_{Substrate}$. During substrate heating, the substrate is nearly isothermal and we assume $T_{Substrate} = T_{Surface} = T_{Interface}$. The separate experiments generate two linear equations for each type of substrate: $V_{TC} = C_1 T_{Interface}$ and $V_{TC} = C_2 T_{Heater}$, where C_1 is thermopower induced by the temperature increase of the interface and C_2 is thermopower induced by the temperature increase of the cantilever heater. We combine these equations to eliminate the variable V_{TC}. The constants are $C_{1,Glass} = 3.16\ \mu$V K^{-1}, $C_{1,Quartz} = 3.62\ \mu$V K^{-1}, $C_{2,Glass} = 1.81\ \mu$V K^{-1}, and $C_{2,Quartz} = 0.43\ \mu$V K^{-1}. It is thus possible to extract the tip–substrate interface temperature $T_{Interface} = (C_2/C_1)T_{Heater}$.

Figure 6 shows $T_{Interface}$ as a function of T_{Heater} for both substrates. The non-dimensional interface temperature, $\theta_{Interface} = (T_{Interface} - T_\infty)/(T_{Heater} - T_\infty)$, is the slope of a linear fit to the experimental data. The potential for heat transfer is represented by the excess temperature between a region of the heated cantilever, $T_{Interface}$ or T_{Heater}, and the temperature of the ambient environment, T_∞. In this case, T_∞ is room temperature. For a heated tip contacting a room temperature substrate in air, $\theta_{Interface,Glass} = 0.593$ and $\theta_{Interface,Quartz} = 0.125$. The substrate thermal conductivity limits efficient heating of the tip–substrate interface; as the thermal conductivity of the substrate increases, the temperature rise at the interface decreases for a constant heater temperature. Simply increasing the thermal conductivity of the substrate from 1.1 to 9.4 W m^{-1} K^{-1} requires a 5× increase in the cantilever heater temperature to reach the same interface temperature. In order to generate a large value of $T_{Interface}$ for a substrate having high thermal conductivity, either T_{Heater} must be large or a thin thermal insulating layer must be prepared on the substrate surface.

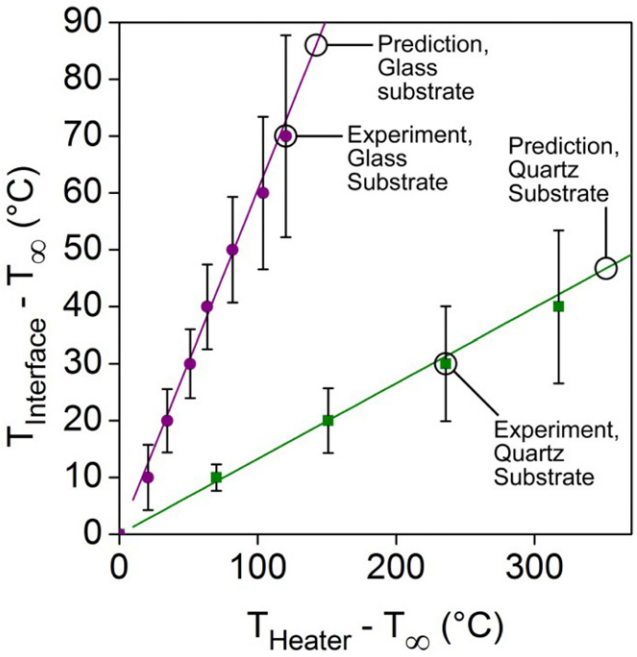

Figure 6. Measurements and simulations for tip–substrate interface temperature as a function of cantilever heater temperature. The substrate was either soda-lime glass or quartz. The linear slopes represent the non-dimensional temperature $\theta_{Interface} = (T_{Interface} - T_\infty)/(T_{Heater} - T_\infty)$.

5. Modeling and analysis

To help understand the tip–substrate interface temperature, we consider a thermal resistance network to relate cantilever heater temperature to tip–substrate interface temperature [4, 11, 12]. Figure 6 shows the predicted interface temperature relationship using this resistance network model for glass and quartz substrates. Figure 7 shows the thermal circuit used to model the relative tip–substrate interface temperature, $\theta_{Interface}$, as a function of cantilever heater temperature, θ_{Heater}. The temperature drop from θ_{Heater} to $\theta_{Interface}$ depends on the relative sizes of the thermal resistances in the heat flow system, especially the interfacial contact resistance, $R_{Contact}$, and thermal resistance of the substrate, R_{Sub}.

There are three conduction modes for dissipation of heat generated in the resistive region near the tip: through the silicon cantilever legs, through the gap between cantilever and substrate, and through the silicon cantilever tip to the substrate. There is negligible convective heat transfer between the cantilever and air due to the high surface area to volume ratio and lack of air motion [36]. Heat conduction through the air slightly raises the surface temperature, $\theta_{Surface}$, in the general vicinity of the tip, and conduction through the tip further raises the local temperature at the tip–substrate interface, $\theta_{Interface}$. Thermal resistance through the air gap, R_{gap}, is treated as one-dimensional conduction through air. The thermal resistance of the substrate beneath the air gap is

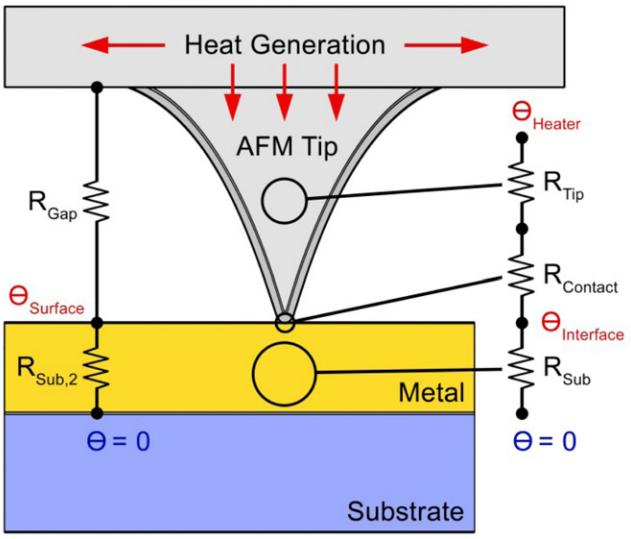

Figure 7. Thermal circuit for heat flow through the tip of a heated AFM probe. The heater temperature rise, θ_{Heater}, is calibrated using Raman microspectroscopy and the tip–substrate interface temperature, $\theta_{\text{Interface}}$, is unknown. The relative thermal resistances of the tip, R_{Tip}, interface, R_{Contact}, and substrate, R_{Sub}, determine the relative temperature difference between θ_{Heater} and $\theta_{\text{Interface}}$.

$R_{\text{Sub},2}$. We treat heat flow through the air gap as a circular heat source on a semi-infinite substrate, with diameter equivalent to the cantilever width of 60 μm, to account for heat spreading into the substrate.

Heat flow through the silicon tip is reduced as the cross-sectional area tapers and the thermal conductivity diminishes due to phonon–boundary scattering. Nelson and King treated heat conduction through a silicon tip as two regimes: conduction through a conical tip capped by a hemisphere with radius equal to the radius of curvature of the tip [4]. For simplicity, we consider total tip thermal resistance, R_{Tip}, and use their reported value for thermal resistance of a silicon AFM tip. We estimate tip contact area using the Hertzian model for elastic contact [37]. The circular tip contact area affects the interfacial contact resistance, R_{Contact}, and helps determine heat spreading under the tip. The tip contact radius $a = 1.8$ nm for a platinum-coated tip of radius 50 nm pressing into a gold-coated substrate with an applied force of 10 nN. Heat flow from the tip contact area into the substrate is treated as a circular heat source with diameter $2a$ in contact with a flat, semi-infinite substrate.

Table 1 shows calculated resistances for the thermal resistor model. We used R_{Contact} as a fitting parameter because quantitatively determining this value is beyond the scope of this work; the contact resistance is examined in more detail elsewhere [5, 6, 11, 38]. A value of 10^8 K W^{-1} for R_{Contact} yields good agreement between model and experiment, and is close to published results reporting tip–substrate contact resistance [4–6, 11, 38]. In comparison, Gundrum *et al* report that the thermal conductance of a metal–metal interface is of the order of 10^9 W m^{-2} K^{-1}, which yields a comparable thermal contact resistance of 10^8 K W^{-1} for our tip contact area. The thermal resistance between the tip and the substrate, R_{Contact}, and the resistance of the substrate, R_{Sub}, are the largest resistances in this system by at least an order of magnitude, and so these resistances govern heat flow through the tip. The order of magnitude difference in substrate thermal resistances stems from the difference in substrate thermal conductivities and is primarily responsible for the difference in tip–substrate interface temperatures across materials.

Table 1. Network model thermal resistances.

	Glass substrate (K W^{-1})	Quartz substrate (K W^{-1})
R_{Tip}	1.0×10^{6}[a]	1.0×10^{6}[a]
R_{Contact}	1.0×10^{8}	1.0×10^{8}
R_{Sub}	1.3×10^{8}	1.5×10^{7}
R_{Gap}	1.4×10^{5}	1.4×10^{5}
$R_{\text{Sub},2}$	7.6×10^{3}	8.9×10^{2}

[a] From reference [4].

6. Conclusion

We have demonstrated temperature-dependent electronic measurement of thermoelectric voltage using a single AFM cantilever. The electro-thermal cantilever facilitates simultaneous tip-side heating of a sample and determination of tip–substrate interface temperature using a point contact thermocouple. The interface temperature is directly measured as a function of cantilever heater temperature, which circumvents the need for calibration on temperature-sensitive materials requiring constant tip–substrate thermal conductance. This interface temperature calibration method is appropriate for substrates with thermal conductivity < 20 W m^{-1} K^{-1}.

In conclusion, we have studied the tip–substrate interface temperature between a heated cantilever and a substrate using the thermoelectric point contact at the tip of an electro-thermal cantilever. When the cantilever is heated, the non-dimensional interface temperature is 0.593 for soda-lime glass and 0.125 for quartz. The measurements match well with a model that assumes the tip–substrate interface contact resistance is 10^8 K W^{-1}. This work could improve nanometer-scale temperature measurements and applications of heated AFM cantilevers.

Acknowledgment

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