Quantum Dots at Room Temperature Carved out from Few-Layer Graphene

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S *Supporting Information*

ABSTRACT: We present graphene quantum dots endowed with addition energies as large as 1.6 eV, fabricated by the controlled rupture of a graphene sheet subjected to a large electron current in air. The size of the quantum dot islands is estimated to be in the 1 nm range. The large addition energies allow for Coulomb blockade at room temperature, with possible application to single-electron devices.

KEYWORDS: *Graphene, quantum dots, quantum transport, single-electron transistors, molecular transport*
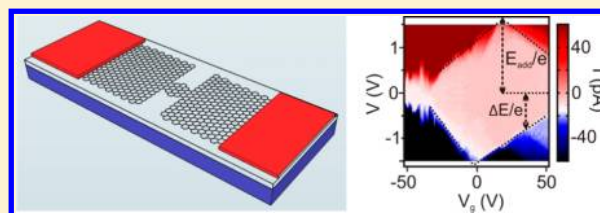
Graphene is a one-atom-thick planar sheet of sp²-bonded carbon atoms whose shape can be structured by means of standard top-down fabrication techniques, representing a simple and scalable approach to realize electronic devices. Indeed, one of the most appealing research directions involving graphene is its use as the base material for electronic circuitry that is envisaged to consist of nanometer-sized elements.[1,2] For this purpose, graphene nanoribbons have captured widespread attention.[3−11] Also, quantum dot (QD) devices made entirely from graphene are considered, with possible applications to single-electron transistors and supersensitive electrometry.[12,13]

Most QDs reported to date operate at cryogenic temperatures, which limits their use in applications. In practice, the two most important conditions for room-temperature operation are addition energies much larger than the thermal energy at 300 K, i.e., ≫26 meV, and stable device operation. Individual molecules in between two electrical contacts can act as quantum dots, and addition energies are usually in excess of 100 meV.[14−16] Nevertheless, the operation of molecular devices at room temperature is often limited due to the high atomic mobility of the metallic electrodes which renders them unstable at room temperature.[17] Recently, it was reported that single P atoms in a Si lattice act as QDs, but room-temperature operation remains to be demonstrated.[18] Room-temperature QDs and single-electron transistors have been realized in ultrasmall metallic grains,[19] and in etched silicon devices.[20,21] Furthermore, RT-QDs have been achieved within an individual metallic carbon nanotube (CNT), by introducing a kink in individual CNTs by atomic force microscopy (AFM) manipulation.[22] However, it was not possible to completely suppress the current at room temperature due to thermal smearing. Furthermore, these CNT RT-QDs are not easy to fabricate and cannot easily be scaled up to form QD arrays.

Here, we report a simple method to fabricate all-graphene quantum dots that can operate at room temperature. These graphene QDs are endowed with addition energies (E_{add}) that

can be as large as 1.6 eV. Their formation relies on the controlled rupture of a few-layer graphene sheet subjected to a large electron current. Simple estimates show that the size of the charge-carrier island of these quantum dots lies in the 1 nm range.

We start by briefly describing our fabrication technique. Few-layer graphene flakes (between 3 and 18 nm thick) are deposited by mechanical exfoliation of kish graphite (Toshiba Ceramics) on degenerately doped silicon substrates coated with 280 nm of thermal silicon oxide. For the exfoliation, we use standard wafer protection tape, as it leaves little adhesive residue on substrates. Electrodes are patterned on top of selected few-layer graphene flakes by electron-beam lithography and subsequent Cr/Au evaporation, followed by lift-off in cold acetone and dichloroethane. Initial device resistances at low bias are in the order of 200 Ω to 3 kΩ.

We now proceed to the formation of quantum dot devices by electroburning in air,[23−25] using a similar technique to the one reported for current-annealing of graphene,[26,27] or the controlled rupture of shells of multiwall carbon nanotubes.[28−30]

Typically, a voltage (V) ramp is applied to the few-layer graphene flake (1 V/s), while the current (I) is continuously recorded with 200 μs sampling intervals. The variations in the conductance ($G = I/V$) are monitored, with a feedback condition set at a >10% drop in G within the past 200 mV of the ramp. Upon the occurrence of such a drop, the voltage is swept back to zero in 100 μs. Immediately after, a new sweep starts from zero voltage and the process is repeated, in this way gradually narrowing down the flake (see Figure S1 in the Supporting Information). The process can be repeated until a nanometer spaced gap is formed.[24] Just before the formation of a nanogap, a very narrow connection is left between the two bigger parts of the flake,[25] forming either a single quantum dot

or several quantum dots in series (see Figure S2 in the Supporting Information). Figure 1 shows a schematic of a nanometer-sized quantum dot carved out of a graphene sheet by electroburning and an AFM image of a typical device.
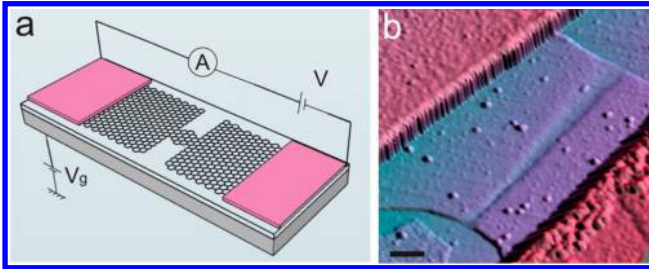

Figure 1. (a) Schematic of the device and measurement setup. (b) AFM image of a typical device.[31] A gap is formed via electroburning, separating the few-layer graphene flake into two parts which can be connected through a connection so tiny that it cannot be imaged by AFM. Remarkably, this tiny connection can form a single quantum dot with addition energies as large as 1.6 eV. The scale bar is 400 nm.

When the two-point resistance at zero gate voltage (V_g) at 100 mV source-drain voltage (V) exceeds 100 MΩ, the feedback controlled electroburning is stopped and stability diagrams as a function of V_g and V are taken to determine if several dots in series or a single dot were formed (more details are given below). If several quantum dots in series are found, the electro-burning procedure can be applied once again in order to obtain a single dot. The fabrication technique has a reasonable yield: out of 36 devices studied, 9 exhibited single quantum dot behavior, 11 showed signatures of QDs coupled in series, and 13 were burned through completely, forming open gaps between the two electrodes. See Table S1 in the Supporting Information for details of the properties of the fabricated single-dot devices.

In the devices exhibiting quantum-dot behavior, we find that the conductance G of the graphene sheet at low source-drain bias is a strong function of the back gate voltage (V_g), showing Coulomb peaks in some cases. Measuring the current (I) as a function of source-drain bias (V) and V_g can yield well-defined Coulomb diamonds for some devices, which indicate the presence of charge carrier islands in the ultranarrow constriction. Figures 2, 3, and 4 (and Figures S3 and S4 in the Supporting Information) display typical examples of such Coulomb diamonds, measured in different samples at $T = 10$ K or at room temperature. In Figure 2a, the diamond is closed, which is usually a sign that a single island is formed. Note that, unfortunately, we were not able to record multiple Coulomb diamonds on most samples, because it was not possible to sweep the gate to larger positive or negative values due to the limit set by the electrical breakdown of our SiO_2 gate dielectric (typically ∼60 V). Nevertheless, for some samples, we were able to resolve more than two halves of the Coulomb diamonds with similar heights (see Figure 4), thus demonstrating that not narrow constrictions but quantum dots were formed. Indeed, a nanoribbon would give rise to a real bandgap,[32−34] in which case a single region of suppressed current is expected.

In the Coulomb blockade regime, the diamond's height along the V-axis is a measure of the energy, E_{add}, needed to add one charge carrier to the island. The addition energies we measure have strikingly large values, up to 1.6 eV; see Figure 2a. The value of 1.6 eV is approximately 1 order of magnitude larger
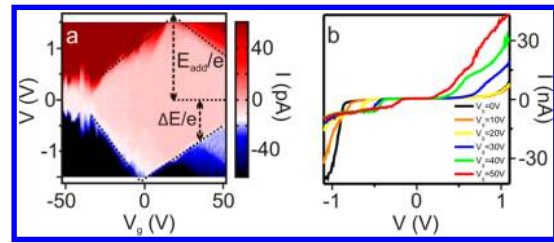

Figure 2. Large addition energy quantum dots at 10 K. (a) Current map of sample 1 in Table S1 (Supporting Information) as a function of the applied bias voltage V_b and gate voltage V_g from which $E_{add} \sim 1.6$ eV can be extracted. The noise centered at $V_g \sim -40$ V could possibly have resulted from an environmental charge instability or could also have resulted from a second (larger) disorder-induced island. On the lower right side, a stepwise increase of the current due to an excited state entering the bias window can be observed. A quantized level spacing of $\Delta E \sim 0.8$ eV can be extracted. The fact that the excited level is only visible on one side of the Coulomb diamond (in this case at negative voltage) can be attributed to an asymmetry in the coupling to the leads.[35,36] (b) Current−voltage traces at various V_g for device 2 in Table S1 (Supporting Information). The stepwise increase of the current is due to an excited state entering the bias window, thereby increasing the probability for electrons to pass through the island. The full stability diagram of this device is shown in Figure S3 (Supporting Information).[37]
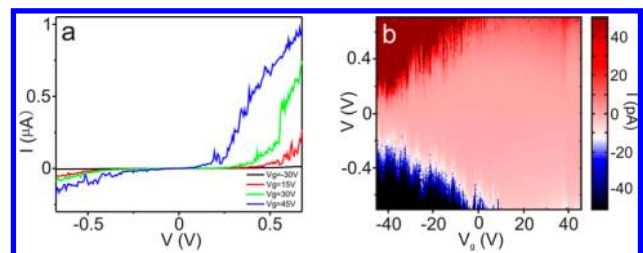

Figure 3. Room-temperature operation of graphene quantum dots (device 5 in Table S1, Supporting Information).[37] (a) $I-V$ traces for four different gate voltages. (b) Current map as a function of V_g and V; the conductance is fully suppressed over a large gate-voltage range (over 50 V).
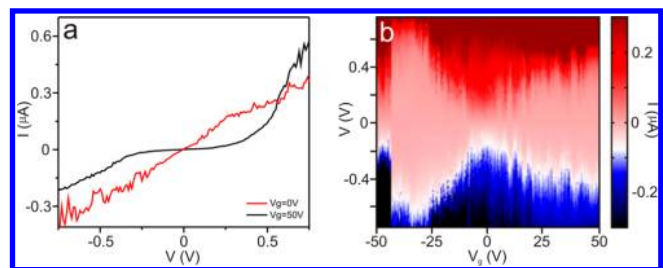

Figure 4. Room temperature operation of quantum dots (sample 4 in Table S1, Supporting Information).[37] (a) $I-V$ traces taken at $V_g = 0$ V (red) and $V_g = 50$ V (black). (b) Current map as a function of V_g and V at room temperature. Two diamond-shaped regions of suppressed current can be observed. The jump at $V_g = -45$ V probably originates from an environmental charge instability.

than E_{add} in the largest addition energy graphene single electron transistors reported so far.[13,23]

Apart from the addition energy, Figure 2 gives information on the quantized level spacing (ΔE), the energy difference between consecutive discrete orbitals on the islands. When not only the ground state but also an excited state electrochemical potential falls inside the bias window, there are two transport

channels through the dot instead of just one. This increases the probability for electrons to pass through the island and gives rise to a stepwise increase of the current (see Figure 2). In Figure 2a, ΔE is approximately 0.8 eV, assuming that no excitations occur below 0.4 eV. From ΔE and E_{add}, the charging energy can be extracted, $2E_c = e^2/C_T = E_{add} - \Delta E \sim 0.8$ eV, where C_T is the total capacitance of the dot. In contrast to earlier reports,[13] we thus find that E_c cannot be neglected even for ultrasmall graphene islands.

It is surprising that, without intentionally introducing tunnelling barriers between the graphene electrodes and the charge carrier island, confinement strong enough for quantum dot formation takes place. In patterned graphene quantum dots, two constrictions in series are defined lithographically, creating a small island in between.[13,38] In our case, it is unlikely that two similar or even narrower constrictions forming an island in between have formed unintentionally, nor has it been observed on suspended devices formed by a similar mechanism.[23,25] Quantum dot formation has been observed in graphene nanoribbons on a SiO_2 substrate and was ascribed to a quantum confinement energy gap combined with edge disorder and charge inhomogeneities in the SiO_2 which give rise to charge puddles.[38−40] We do not believe our quantum dots result from charge inhomogeneities in the substrate because quantum dot formation by electroburning was also observed in suspended samples.[23] In the latter case, island formation was ascribed to charge carriers becoming localized by potential fluctuations along the ultranarrow constriction in the presence of a confinement gap due to, e.g., molecules having reacted with the dangling bonds.[23] More generally, any type of edge disorder could be responsible for localization of charges and island formation.

We now turn to estimating the size of our smallest quantum dot, namely, the one measured in Figure 2a. The level spacing ΔE is approximately 0.8 eV and can be used to estimate the island size. Using the band structure of monolayer graphene and a square confinement potential, the diameter of the carrier island can be estimated according to $d = \pi \hbar v_F / \Delta E \sim 2.6$ nm. Here, $v_F \sim 10^6$ m/s is the Fermi velocity and $\hbar = 6.582 \times 10^{-16}$ eV·s is the reduced Planck constant. Since we cannot exclude that the dot is formed from bilayer graphene, we also estimate the size of the dot using the band structure of bilayer graphene and a square potential and obtain $d = (\hbar^2 \pi / m^* \cdot \Delta E)^{1/2} \sim 3$ nm, where $m^* \sim 0.033 m_e$ is the effective mass in bilayer graphene (m_e is the electron mass),[41] and obtain a similar value as that for monolayer graphene.

A second independent estimate of the size of the graphene charge carrier island can be obtained from the charging energy of the dot $E_c = e^2/2(C_G + C_D + C_S + C_{self}) \sim 0.4$ eV, where C_S and C_D are the capacitances to the source and drain, respectively, and C_{self} is the self-capacitance of the carrier island of the quantum dot. From the stability diagram in Figure 2a, we can extract the values $C_G = 1.66 \times 10^{-21}$ F, $C_S = 4.15 \times 10^{-20}$ F, and $C_D = 5.76 \times 10^{-20}$ F.[27] Calculating $C_T = C_G + C_D + C_S + C_{self} = e^2/2E_C \sim 2 \times 10^{-19}$ F, we see that the total capacitance is mostly given by C_{self}. We approximate $C_T \sim C_{self}$ to obtain a further estimate of the size of the carrier island by modeling it as a circular disk of diameter d, for which $d = e^2/4 \cdot \varepsilon_0 \cdot (\varepsilon_r + 1) \cdot E_c$, with ε_0 the vacuum permittivity and $\varepsilon_r = 3.9$ the relative dielectric constant of SiO_2. This approach gives $d = 2.26$ nm.

Another rough estimate of the island size can be obtained from the back gate capacitance. We can estimate the dot

diameter from C_g by looking at two extreme scenarios. One model is that of a parallel plate capacitor, and the other one corresponds to a small disk above an infinite plane (no screening from the electrodes). Using the formula for a parallel plate capacitor $C_g = \varepsilon_0 \cdot \varepsilon_r \cdot \pi \cdot (d/2)^2/D$, where $D = 285$ nm is the thickness of the SiO_2, we obtain $d \sim 4$ nm. For a small disk on an infinite plane, the capacitance is given by $C_g = \varepsilon_0 \cdot (1 + \varepsilon_r) \cdot 2d$,[42] resulting in $d \sim 0.018$ nm. Due to screening by the electrodes, most of the back gate area does not contribute to the capacitance to the island, so the latter estimate is far off. Taking for illustration purposes the capacitance of the island to a 7 nm diameter disc located 285 nm underneath, the island size would again be $d \sim 1$ nm.

Overall, the measurements suggest that the diameter of the island of the quantum dot displayed in Figure 2a is on the 1 nm scale.

To put these results in perspective, the charging energy $E_c \sim 0.4$ eV in even our smallest quantum dot is almost 1 order of magnitude bigger than the value $E_c \sim 50$ meV of a quantum dot consisting of a single phosphorus atom in a Si substrate, which corresponds to the binding energy of an isolated phosphorus donor in bulk silicon.[18,43] As a matter of comparison, the diameter of a phosphorus dopant (d_P) in Si corresponds to twice its effective Bohr radius (r_{eB}) which can be estimated according to $d_P = 2r_{eB} = 4.4$ nm,[44] in this case with a spherical symmetry instead of a disk shape.

Importantly, we are able to measure Coulomb blockade even at room temperature, see Figures 3 and 4, and not only single $I-V$ traces but also stability diagrams which are stable over large ranges in V_g and V. The device in Figure 3 appears completely insulating with no measurable conductance over an extended range of V_g (>50 V). Room-temperature operation is possible because E_c and ΔE, and consequently also E_{add}, in our devices are much bigger than the thermal energy $k_B T$, which at $T = 300$ K corresponds to 25.6 meV. Moreover, the stability of graphene at elevated temperatures due to its strong sp^2 bonds is another important factor to enable room temperature operation of our quantum dots.

Nevertheless, in all the quantum dots measured at room temperature, more noise is present in the data as compared to the measurements taken at low temperature; see Figures 3 and 4. Apart from that, sudden jumps in V_g sometimes occur while taking full stability diagrams, as illustrated in Figure 4. These limitations in device performance are likely to be set by nearby dopants and trapped charges, for example, in the silicon oxide, that are mobile at room temperature. We believe that these factors, extrinsic to the graphene island, are the likely origin of the noise and scatter present in Figures 3 and 4.[44,45] Indeed, the motion of a single dopant could alter the dielectric environment and therefore the current through the QDs. Another possible source of noise could be the thermally activated motion of polar dangling bonds in the vicinity of the quantum dot which could possibly also modify the dielectric environment.[46] Also, the switching events such as the one occurring in Figure 4 at $V_g \approx -45$ V are likely to be caused by trapped charges moving in the dielectric silicon oxide layer. The trapped charges are more mobile at room temperature and can result in sudden jumps, causing switches of the electrostatic environment, which in turn lead to sudden jumps in the current through the graphene quantum dot. Indeed, the presence of just one dopant can alter the performance of short-channel transistors depending on where they are located.[44] Possibly, a gate dielectric with only few trapped charges, such as hBN,[47] could be used to reliably

operate these devices without random changes in the dielectric environment, thereby reducing the noise and switching events present in the current data.

In conclusion, we have shown that the rupture of a graphene sheet subjected to a large current can be harnessed to fabricate graphene quantum dots where the active component is very close to the ultimate physical limit of Moore's law. The as-fabricated quantum dots are endowed with addition energies as large as 1.6 eV. We estimate the size of the carrier island of the quantum dots to lie in the 1 nm range. Remarkably, graphene remains stable and conductive at the nanometer scale and the observed large addition energies give rise to Coulomb blockade at room temperature, a prerequisite for most applications. We further note that the fabrication technique is not limited to the use of exfoliated graphene but could also be applied to CVD-grown few-layer graphene over large areas, paving the path to more complex, integrated devices involving multiple QD devices integrated on the same chip.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Further details about the electroburning procedure, a table with the properties of all the fabricated single dot devices, data of quantum dots in series, further measurements of the devices in Figure 2b, as well as data of other large addition energy quantum dots both at low and at room temperature. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes
The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

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