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Ambient-Processable High Capacitance Hafnia-Organic Self-Assembled Nanodielectrics

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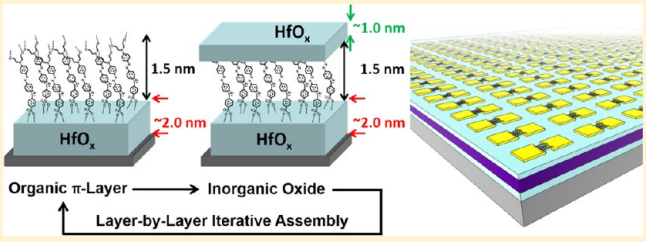
Supporting Information

ABSTRACT: Ambient and solution-processable, low-leakage, high capacitance gate dielectrics are of great interest for advances in low-cost, flexible, thin-film transistor circuitry. Here we report a new hafnium oxide-organic self-assembled nanodielectric (Hf-SAND) material consisting of regular, alternating π-electron layers of 4-[[4-[bis(2-hydroxyethyl)-amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]-pyridinium bromide) (PAE) and HfO_2 nanolayers. These Hf-SAND multilayers are grown from solution in ambient with processing temperatures ≤150 °C and are characterized by AFM, XPS, X-ray reflectivity (2.3 nm repeat spacing), X-ray fluorescence, cross-sectional TEM, and capacitance measurements. The latter yield the largest capacitance to date (1.1 μF/cm^2) for a solid-state solution-processed hybrid inorganic−organic gate dielectric, with effective oxide thickness values as low as 3.1 nm and have gate leakage <10^{-7} A/cm^2 at ±2 MV/cm using photolithographically patterned contacts (0.04 mm^2). The sizable Hf-SAND capacitances are attributed to relatively large PAE coverages on the HfO_2 layers, confirmed by X-ray reflectivity and X-ray fluorescence. Random network semiconductor-enriched single-walled carbon nanotube transistors were used to test Hf-SAND utility in electronics and afforded record on-state transconductances (5.5 mS) at large on:off current ratios (I_{ON}:I_{OFF}) of ∼10^5 with steep 150 mV/dec subthreshold swings and intrinsic field-effect mobilities up to 137 cm^2/(V s). Large-area devices (>0.2 mm^2) on Hf-SAND (6.5 nm thick) achieve mA on currents at ultralow gate voltages (<1 V) with low gate leakage (<2 nA), highlighting the defect-free and conformal nature of this nanodielectric. High-temperature annealing in ambient (400 °C) has limited impact on Hf-SAND leakage densities (<10^{-6} A/cm^2 at ±2 V) and enhances Hf-SAND multilayer capacitance densities to nearly 1 μF/cm^2, demonstrating excellent compatibility with device postprocessing methodologies. These results represent a significant advance in hybrid organic−inorganic dielectric materials and suggest synthetic routes to even higher capacitance materials useful for unconventional electronics.



INTRODUCTION

For decades, silicon dioxide has dominated electronics technologies as the standard gate dielectric material in complementary metal oxide semiconductor (CMOS) integrated circuits due to its excellent compatibility with the silicon semiconductor.[1] However, recent advances in semiconductor performance afforded by materials such as graphene,[2] carbon nanotubes,[3] and metal oxides[4] require corresponding advances in compatible gate dielectric materials. Such materials must exhibit very large capacitance, high breakdown strength, low parasitic current leakage, low trap density, and high thermal stability. Other desirable attributes include amenability to solution or alternative low-cost fabrication methods and compatibility with arbitrary substrates (cloth, plastics, glass, etc.). Generally, SiO_2 fails to satisfy many of these requirements and its relatively low dielectric constant compromises optimal device performance. Charged SiO_2 oxide impurities also lead to unacceptably large levels of transistor drain current (I_d) versus gate voltage (V_g) mismatch in the forward and reverse gate bias sweeps, termed I_d−V_g hysteresis, which precludes predictable and stable performance in logic or integrated circuit applications.[5] This I_d−V_g hysteresis is especially problematic in one-dimensional nanomaterials, such as carbon nanotubes, where efficient charge injection-based trapping has been observed at dielectric−semiconductor interfaces.[6] High k oxide dielectric films, such as hafnia (HfO_2) with k = 25 grown by atomic layer deposition (ALD), have successfully replaced SiO_2 in modern silicon-based CMOS.[7] However, the use of high temperatures (especially in postdeposition annealing)[8] and reactive ALD precursors makes this growth methodology generally unsuitable for new classes of substrates

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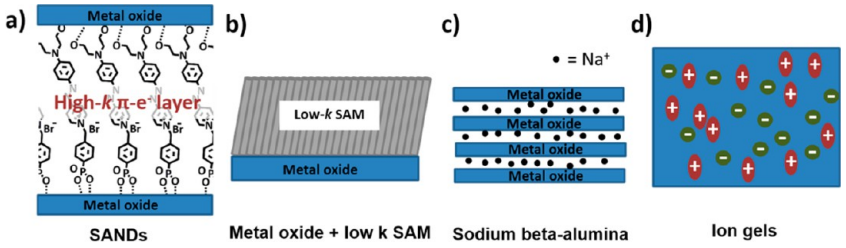

Figure 1. Examples of unconventional gate dielectric materials reported in the recent literature.[15a−h,12,15i]

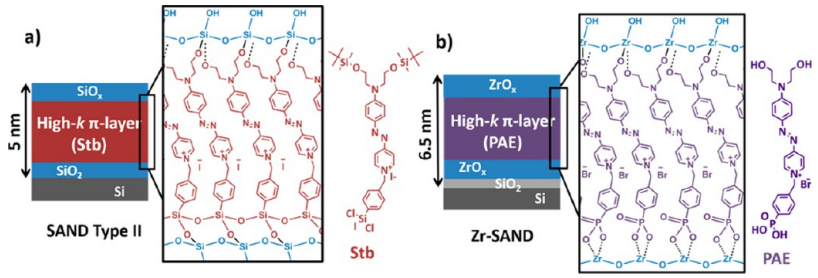

Figure 2. SAND gate dielectric structures. (a) Halosilane-derived type II SAND;[15i] and (b) zirconia-phosphonate-derived Zr-SAND.[15a] PAE = 4-[[4-[bis(2-hydroxyethyl)-amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]pyridinium bromide.

or organic and nanostructured semiconductors envisioned for next-generation electronics.

Solution-based gate dielectric film deposition performed at low temperatures, on the other hand, offers the possibility of large-area fabrication of electronic circuitry on flexible and transparent polymeric substrates which are low in cost but cannot sustain high processing temperatures.[9] This approach might enable access to high-quality dielectrics from straightforward low-cost routes on disparate substrates.[10a,9b,10b,c] The majority of alternative bottom-up fabrication routes for high-performance gate dielectrics that compete with ALD include sol−gel solution processing and molecular self-assembly, or a combination thereof (Figures 1a,b).[11] Several research groups have combined ALD with self-assembly processes to realize promising low-leakage, high-capacitance bilayer structures,[12] while others have used self-assembled monolayers (SAMs) in conjunction with plasma oxidized metal electrodes (Figure 1b),[13] however reports with low temperature, all-solution process approaches are far more limited.[13b,e,12,14] Although the field has grown rapidly in recent years, routes beyond bilayers to produce functional multilayers or superlattice structures, have remained challenging.

Today, several solution-processing approaches to gate dielectric films combine some form of high-k inorganic oxide with a low-k saturated organic SAM (Figure 1b).[16,13b] However, the addition of the organic layer typically compromises the attainable capacitance due to the low relative permittivities (k = ~2.5) exhibited by aliphatic carbon backbones.[15i,17] Recognizing the inherent drawbacks of using low-k hydrocarbon SAMs on the overall capacitance and leakage in SAM/SAM-metal oxide gate dielectrics, this laboratory previously developed a highly polarizable stilbazolium-based π-layer (Stb, PAE) as an alternative component for hybrid organic−inorganic self-assembled nanodielectrics (SANDs), which exhibit promising device properties and capacitance (Figures 1a and 2).[15a,18,15i] The key to SAND performance over simple solution-processed oxides is the interleaving of high-k Stb-derived layers ($k \approx 16$) in an alternating fashion between oxide nanolayers, which enhances the overall k, minimizes leakage, and helps offset chemical/electrical defects, such as pin-holes within the oxide layers. The original assembly chemistry employed reactive iododichlorosilane linkages (Figure 2a) which are tailored for covalently linking to oxide surfaces (e.g., Si/SiO_2, Al/Al_2O_3).[15i] Therefore, in an effort to develop more user-friendly, ambient processable SAND variants, phosphonic acid linkages (Figure 2b) which can be applied widely to metal oxide surfaces, such as those of alumina, zirconia, and hafnia, were introduced.[19] Early zirconia-based SANDs (Zr-SANDs) attained promising capacitance densities of ~0.750 $\mu F/cm^2$ at the single layer limit,[15a] while the best reported bilayer metal oxide-SAM systems (Figure 1b) generally achieve capacitances in the 0.5−0.75 $\mu F/cm^2$ range.[16,15c−e,13a,c−e,12,20,17a] An approach utilizing short-chain (sub-1 nm thickness) SAMs on plasma oxidized metals reported capacitance densities up to ~1.75 $\mu F/cm^2$, but these are not processed entirely from solution, and the reported device performance (TFT metrics, leakage, interfacial roughness) does not equal those of the thicker, lower capacitance (sub-1 $\mu F/cm^2$) homologues.[13a] Capacitances in excess of 1 $\mu F/cm^2$ with well controlled leakage profiles[15a,16,20] have not to date been achieved with superlattice gate dielectrics processed from solution.

There has been progress, however, utilizing hafnia + phosphonic acid SAMs as gate dielectrics, most notably from Jen,[15c−e] however these approaches require high-temperature annealing of the spun-cast oxide (600 °C) prior to self-assembly of the organic layer and typically require long SAM formation times (>12 h) to produce well-packed monolayers. Capacitance densities greater than 0.6 $\mu F/cm^2$ are seldom attained.[15c,16,15d,e,12,20] Note that sodium β-alumina gate dielectrics[15b,f] (Figure 1c) and solution processed ion gel materials[21,15g] (Figure 1d) have achieved capacitance densities greater than 1 $\mu F/cm^2$, but such systems rely on mobile ions for the large capacitance, which may be frequency and temperature dependent, and the materials may not always be solids at room temperature and above. The reports[15f] on sodium β-alumina ($Na-Al_2O_3$) multilayers also indicate that high-temperature annealing (>700 °C) is required for stable low-leakage

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performance, implying incompatibility with roll-to-roll processing, organic semiconductors, and low-cost plastic substrates.

The goal of the present research effort is to develop enhanced performance hybrid superlattice dielectrics using alternative oxides as the SAND oxide component (Figure 1a). The motivation for extending to hafnia is based on reports indicating differential affinity of phosphonic acids for various oxides versus ZrO_2,[22] along with HfO_2 thermodynamic and surface chemical differences that may beneficially affect the dielectric properties at low process temperatures.[19,23] In this contribution we report on the growth, structural and electrical characterization, and TFT implementation of a novel hafnia-based self-assembled nanodielectric (Hf-SAND), fabricated entirely from solution at low temperatures ($\leq$150 °C) and in ambient atmosphere. These hybrid organic−inorganic superlattice structures are characterized by a number of compositional, structural, and electrical techniques and are shown to exhibit high structural regularity at the nm level, very high capacitances (>1 μF/cm^2), low leakage (10^{-7} A/cm^2 at ±2 MV/cm), and very high thermal stability. Moreover, purified single-wall carbon nanotube-based TFTs fabricated with the new Hf-SANDs as gate dielectrics exhibit record on-state transconductance (5.5 mS) and other state-of-the-art performance metrics.

EXPERIMENTAL SECTION

General Methods. All reagents were sourced from Sigma-Aldrich unless otherwise noted. n^{++} silicon wafers (⟨100⟩, 0−0.018 Ω·cm resistivity) were purchased from WRS Materials and cleaned using piranha solution (3:1 v:v concd H_2SO_4:30% H_2O_2, CAUTION: highly exothermic and oxidizing) immediately prior to dielectric self-assembly. All depositions, cleanings, and wafer handling were carried out inside a Class 10 HEPA-filtered laminar flow preparative clean hood (NuAire) to minimize contamination. The >99% semiconducting single-walled carbon nanotubes (SWCNTs) used for transistor fabrication were first purified by the density gradient ultracentrifugation (DGU) method (see Supporting Information, SI) and collected by vacuum filtration before placement onto the device substrates (Hf-SAND-1). Note that additional detailed descriptions of techniques and characterizations not found below can be found within the SI.

Hf-SAND Growth. The HfO_x sol−gel precursor solution was obtained by first preparing a 73 mM ethanolic solution of $HfCl_4$ under ambient. Concentrated HNO_3 was subsequently added to the cloudy dispersion in a 10:1 molar ratio (HNO_3:$HfCl_4$) as a hydrolysis catalyst. Next, 7 and 15 mM HfO_x solutions were prepared just prior to dielectric self-assembly by simple dilution with ethanol. Substrates were spin coated with an ~15 mM solution of $HfCl_4$ in ethanol (30 s, 5000 rpm) within the NuAire Class 10 HEPA-filtered clean hood. Substrates were baked for a minimum of 30 min at 150 °C to remove solvents and induce film cross-linking/densification. Immediately after baking, the substrates were immersed in a preheated, ~3 mM solution of 4-[[4-[bis(2-hydroxyethyl)amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl) benzyl]pyridinium bromide (PAE)[15a] for 1 h at 60 °C. After rinsing the coated substrates with methanol and blow drying, a ~7 mM solution of $HfCl_4$ in ethanol was spin coated on the substrates (30 s, 5000 rpm) and baked for ~30 min (150 °C) to cap the stilbazolium layer and regenerate the oxide layer for subsequent PAE-HfO_x bilayer growth. Capacitor structures and TFT source-drain electrodes were thermally evaporated by either shadow-mask, or conventional UV photolithography and acetone lift-off.

Atomic Force Microscopy (AFM). All AFM images for surface roughness analysis were collected using a CP-Research (Thermomicroscopes) AFM in air. AFM imaging of the nanotube networks was carried out using a Dimension ICON AFM (Bruker) instrument. Tapping mode AFM was used for imaging pristine dielectric surfaces as well as FET nanotube networks.

X-ray Photoelectron Spectroscopy (XPS). XPS was employed to probe elemental and chemical composition using an Omicron ESCA probe equipped with a monochromated Al Kα X-ray source. An electron flood gun beam energy of 10 eV and an emission current of 0.002 mA were used for charge compensation.

X-ray Reflectivity (XRR). XRR data were acquired using an 18 kW Rigaku ATXG diffractometer. Monochromated X-rays generated from the Cu rotating anode (wavelength λ = 0.1541 nm) were collimated to produce a beam of dimensions 5.0 × 0.1 mm (width × height) with a flux of ~1 × 10^8 photons/s at the sample surface. Electron density profiles were extracted by performing least-squares fits of background-subtracted data to reflectivity curves calculated using the Abeles matrix method.[24]

X-ray Fluorescence (XRF). X-ray florescence data were acquired using an 18 kW Rigaku generator equipped with a Mo rotating anode (wavelength λ = 0.0710 nm). Spectra were acquired using a Vortex silicon-drift diode (SDD) detector (SII Nanotechnology). A clean Si standard was measured for baseline comparison (see SI). Spectra in the range of the Br line (~10 keV to ~13 keV) were fit with multiple peaks and a cubic spline background.

Cross-Sectional Transmission Electron Microscopy (TEM). Cross-sectional TEM samples were imaged using a Hitachi HD-2300A scanning transmission electron microscope with both bright-field and high-angle annular dark-field detectors. The images were taken with the bright-field detector, which has phase contrast.

Hf-SAND Annealing. Unpatterned Hf-SAND substrates were exposed to high-temperature annealing via baking on a hot plate in the dark, but otherwise under ambient laboratory conditions. The hot plate surface temperature was initially set to 150 °C followed by a ramp to either 250 or 400 °C upon placement of the Hf-SAND-coated Si substrates. Samples were baked for a period of 15 or 30 min once the temperature set point was reached and then quickly removed and allowed to cool in room-temperature air. Ti/Au contact pads (150 × 150 μm) were patterned according to the procedures described for the SWCNT TFTs (see SI).

RESULTS AND DISCUSSION

In the following sections, we first discuss the growth of the Hf-SAND superlattice films, followed by characterization of Hf-SAND chemical composition by XPS to assay the presence of hafnium oxide, and utilize the O 1s peak to assess the densification of the sol−gel derived oxide layer. AFM is next used to quantify surface RMS roughness and indicates uniform, pinhole free films, followed by nanostructure characterization by XRR, which reveals smooth, conformal and regularly stacked layers having uniform interlayer spacings. The nanostructural regularity is further confirmed by cross-sectional TEM analysis. Next, electrical properties are measured with metal-insulator-semiconductor (MIS) capacitor devices on polished silicon wafers, which reveal low leakage and large capacitance densities at sub-3 V gate bias, while an XRF Br coverage analysis assays the PAE coverage achieved by the Hf-SAND nanostructures. Finally, bottom-gate, thin-film field-effect transistors are fabricated on Hf-SAND-1 with sorted semiconductor-enriched SWCNTs, and impressive TFT performance is revealed.

Hf-SAND-*n* Film Fabrication. Figure 3 shows the fabrication scheme for the new Hf-SAND-*n* films. Multilayer variants can be prepared by repeating the indicated self-assembly steps in an iterative fashion, where the *n* index (Figure 3) indicates the number of π-electron/HfO_x bilayers grown on top of the initial HfO_x priming layer. XRR measured thicknesses for these hybrid dielectrics are denoted next to the generalized nanostructure illustrated in this figure. Prior to SAND fabrication, degenerately doped, polished Si wafers are carefully cut to avoid particles and cleaned via immersion in piranha solution (3:1 v:v concentrated H_2SO_4:30% H_2O_2) to

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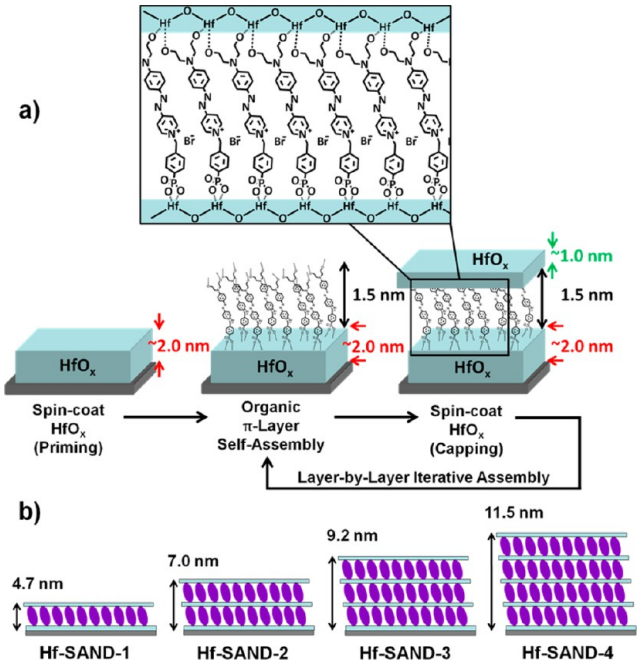

Figure 3. (a) Solution-based Hf-SAND self-assembly procedure employed in this study. (b) Schematic of the various Hf-SAND multilayers produced including the corresponding X-ray reflectivity derived thicknesses (Hf-SAND-1, -4) and estimated thicknesses (Hf-SAND-2, -3).

produce a clean, hydrophilic surface. A thin HfO_x priming layer (2 nm), derived from the $HfCl_4$ precursor, is first spin-coated under ambient and then baked to prepare the wafer surface for phosphonic acid-based self-assembly of the π-electron organic layer (PAE; see Experimental Section and Supporting Information for details). After 60 min immersion in a ~ 3 mM solution of PAE in methanol at 60 °C, the substrates are rinsed with methanol and blown dry with filtered N_2. The resulting HfO_x/π-electron bilayer is then "capped" with a second layer of HfO_x by spin-coating and baking. This process regenerates the metal oxide surface for additional layers (if desired) of phosphonic acid PAE SAM to initiate the next nanodielectric repeat unit.

Surface Morphology and Chemical Characterization of Hf-SAND-*n* Films. Hf-SAND-*n* variants ranging from one to four bilayers (Hf-SAND-1~ −4) were imaged by AFM to quantify the surface roughness, conformality, and contiguity. As depicted in Figure 4, a slight increase in the RMS roughness (~10%) is observed per each added layer. The images are essentially featureless, with these films exhibiting RMS roughness values as low as 1.3 Å for a single layer to 1.7 Å for the four-layer variant, contributing negligible additional roughness to the native oxide Si substrate surface.[25] This modest increase in roughness is consistent with the deposition of additional dielectric layers, while the small magnitude of the increase is likely a reflection of slight structural irregularities. The exceptionally smooth surfaces are ideal for the fabrication of back-gated transistor devices where even moderate interface roughness can detrimentally affect TFT properties, such as carrier mobility, and illustrates the precise level of control afforded by the present processing methodology.[26] The film surface quality is a strong indication of the conformal and uniform coverage of these multilayer dielectric films.

To analyze the elemental and chemical composition of the completed Hf-SAND multilayers, XPS was employed. A survey scan (Figure 5a) reveals dominant photoemission signals from O, Hf, and C. However, no N, Br, or P signals are detected due to the limited relative concentrations in the films and their ≥1 nm depth below the film surface. High-resolution scans of the Hf 4f signal region show a spin−orbit doublet at an energy consistent with the fully oxidized +4 state (Figure 5b),[27] while the O 1s spectrum (Figure 5c) is composed of several peaks. Linear background subtraction and peak fitting results are also shown in Figure 5c. It has been shown that such core-level shifts in the O 1s spectrum are highly sensitive to the relative

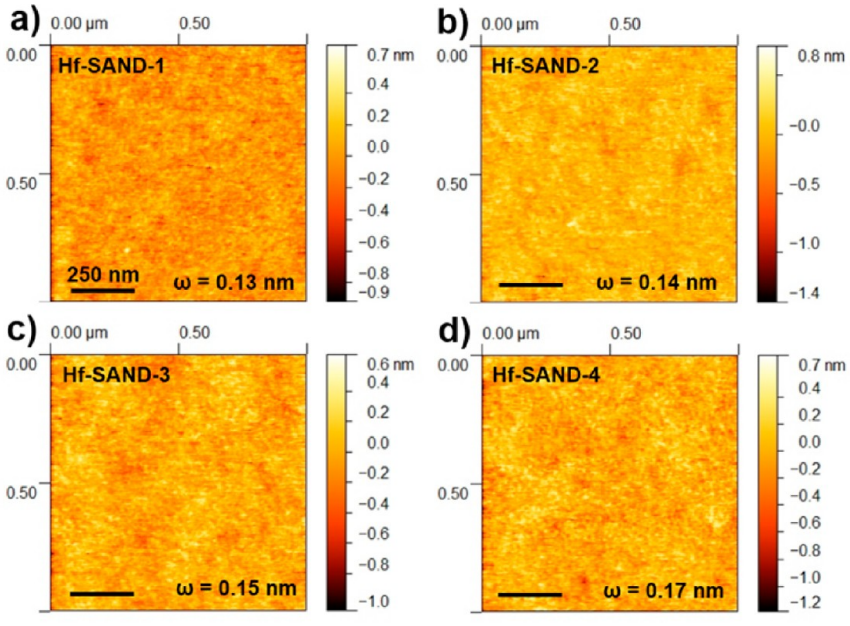

Figure 4. AFM images of monolayer (a) Hf-SAND-1, (b) Hf-SAND-2, (c) Hf-SAND-3, and (d) Hf-SAND-4 systems, and ω indicates the RMS roughness.

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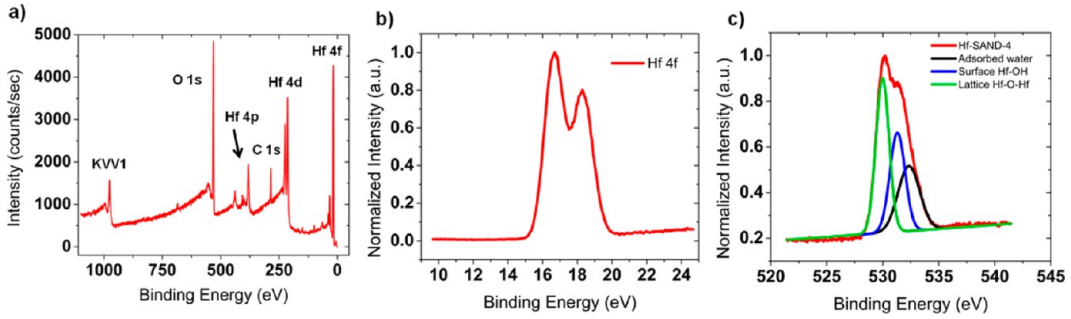

Figure 5. (a) XPS survey scan of a Hf-SAND-1 film. (b) High resolution Hf 4f XPS scan of a Hf-SAND-1 thin film. (c) O 1s XPS of Hf-SAND-4 (red) and the peak fits (green, blue, black) indicating a distribution of known chemical state signatures.

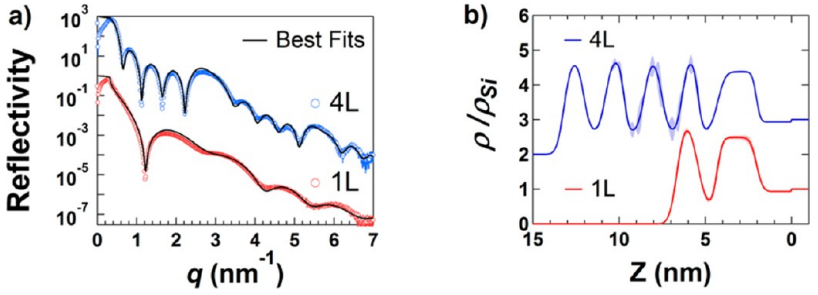

Figure 6. (a) XRR data for Hf-SAND-1 (red) and Hf-SAND-4 (blue, scaled by 10^3) plotted with black lines representing the best fits to the data. (b) Electron density profiles normalized to the density of bulk Si. The red (blue, offset by +2) line corresponds to best-fit reflectivity data for Hf-SAND-1 (Hf-SAND-4). Each result is plotted with a band indicating 1σ uncertainty levels.

degree of M−OH → M−O−M cross-linking in sol−gel processed thin films.[28] The O 1s spectra do exhibit M−OH features, however caution must be exercised due to ambiguity in identifying signals from the hydroxyl groups, which can be attributed to either noncross-linked precursor material within the film (which is expected as a consequence of the low processing temperature) or to surface hydroxyls. Adsorbed water may also dissociate and produce additional surface OH functionalities,[28,23d,29] which are known to readily form on metal oxide surfaces[30] and cause the OH signal to increase over time relative to the HfO_x signal. Because of this complication, quantitative extraction of the degree of cross-linking in sol−gel thin films is challenging, even with an immediate postsynthesis characterization procedure.[31] With this consideration, however, it is nonetheless concluded that the O 1s signal observed after the present 150 °C processing is qualitatively similar to metal oxide spectra of samples processed at much higher temperatures (300 °C)[28] and that the dominant HfO_x peak at 529.88 eV (Figure 5c) indicates an extensively condensed amorphous oxide network.[32] We stress that the amount of noncross-linked OH within the film is still likely non-negligible considering the process temperature, and consequently these films, while dense, are likely not as dense as those of bulk HfO_2. This assertion is further supported by the film electronic properties where the lower effective dielectric constant results from a somewhat lower film density versus that of bulk HfO_2. We conclude that the uniform and small RMS roughness observed by AFM along with the dominant lattice hafnium oxide feature and other compositional details observed by XPS together indicate smooth, chemically homogeneous, relatively condensed HfO_x films.

Hf-SAND-*n* Film X-ray Reflectivity. The quality of the Hf-SAND nanostructures and interlayer ordering was next examined by specular XRR, which is sensitive to the electron density profile of the film in the surface normal direction. The XRR data fit, and the corresponding normalized electron densities (ρ/ρ_{Si}) for one- and four-layer Hf-SAND films are shown in Figure 6. The reflectivity data (Figure 6a) are plotted against the out-of-plane scattering vector $q = 4\pi \sin(\theta)/\lambda$, where θ is the incident beam angle. These data show characteristic oscillations corresponding to a film consisting of layers of alternating high- and low-electron density with smooth (~0.3 nm RMS roughness) interfaces. The first- and second-order diffraction peaks that appear in the 4 L data at q = 2.8 and 5.6 nm^{-1} correspond to a periodicity of $d = 2\pi/q \sim 2.2$ nm. The corresponding best fit values of the electron density profiles are presented in Figure 6b. The 1 L H-SAND sample is found to consist of a 2.2 nm Hf-precursor/primer layer followed by a single 1.3 nm PAE layer and a 1.2 nm HfO_x layer, resulting in a total film thickness of 4.7 nm. The 4 L sample shares the same structural basis as the 1 L but contains four stacked PAE/HfO_2 bilayers and has a total thickness of 11.5 nm. The density of the HfO_x layers is, on average, ~2.6× the electron density of the Si substrate (ρ_{Si}), close to the nominal bulk crystal values[33] where $\rho_{HfO_2} = \sim 2.5\rho_{Si}$ and indicates the presence of relatively dense HfO_x layers atop the PAE layers. The PAE layer itself is found to be only 1.3 nm thick, which is slightly thinner than the expected molecular length if the molecules (1.5 nm) are standing perpendicular to the surface.[15a] This apparent discrepancy is readily explained by a molecular long axis tilt of ~30° with respect to the surface normal, which is typical for SAMs having this type of stilbazolium group assembled on hydroxylated surfaces.[34] From the XRR of Hf-SAND-1 and Hf-SAND-4, a per-layer growth thickness of ~2.3 nm per HfO_x/π-electron organic (PAE) bilayer is extracted, which is identical within experimental error to that derived by XRR for ZrO_2-based Zr-SAND.[15a] By reasonably assuming that the SiO_2 native oxide

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thickness is 1.8 nm,[35] the total thicknesses of Hf-SAND-1 and −4 films on the silicon substrate are estimated to be 4.7 and 11.5 nm, respectively, while interpolated thicknesses for bi- and trilayer variants are then 7.0 and 9.2 nm, respectively. Finally, note that the slight interlayer thickness differences observed in the XRR (Figure 6b) are likely related to the additional thermal processing that is used when subsequent layers are added, which may cause additional densification/contraction of the hafnium oxide.

To further assess the validity of the XRR analysis, a Hf-SAND-4 multilayer film was imaged by cross-sectional TEM (Figure 7). The multilayer structure depicted in earlier Figures 3 and 6b is clearly evident, with very uniform interlayer spacings, which correspond to the alternating organic and inorganic components (also see Figure S8). Note that the thickness of the entire structure observed by TEM approximately corroborates the thickness determined by XRR, which is nominally 11.5 nm for the Hf-SAND-4 construction.

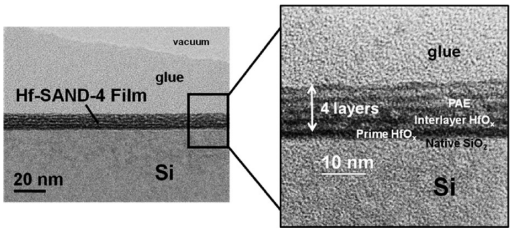

Figure 7. Cross-sectional, bright-field TEM image of a four-layer Hf-SAND structure. Multilayers are visible with uniform spacing and thickness which corroborates the XRR analysis. Note the lighter contrast regions within the multilayers that correspond to the organic PAE film, while the darker regions represent the HfO_x layers. Four layers of alternating organic PAE and HfO_x can be seen, which are depicted by the arrow. The initial HfO_x primer layer comprises the lower most layer directly in contact with the Si native oxide.

Consequently, we conclude that the present fabrication techniques are able to produce highly uniform nanodielectric structures and that the TEM further confirms the structural parameters used for the XRR model.

Electrical Characterization of Metal-(Hf-SAND-*n*)-Silicon Capacitors. In all electronic circuits, it is critical to limit TFT gate dielectric leakage currents for efficient switching and to minimize power consumption during device operation. Of the many methods for evaluating dielectric characteristics, the fabrication of MIS (metal−insulator−semiconductor) structures is straightforward and emulates many of the processing steps expected during transistor fabrication (thermal evaporation, photolithography, lift-off, etc.). In the case of the present capacitor structures, Hf-SAND-*n* dielectric layers (n = 1−4) were deposited on n^{++}-doped polished Si wafers (<0.02 Ω·cm) covered with 1.8 nm native oxide. After Hf-SAND dielectric growth, conventional UV photolithography, and lift-off were utilized to pattern 150 × 150 μm Ti/Au (5 and 50 nm) contacts. Both dielectric leakage and capacitance are obtained by directly probing the top electrode via a two-point probe station and Signatone "cat-whisker" tungsten probes (Figure 8a) and normalized according to the electrode geometry. The measured properties are depicted in Figure 8. The dielectric response of these multilayers can be modeled as a series of parallel plate capacitors according to eq 1, where n represents the number of PAE/HfO_x bilayers (Figure 3) in the sample.

$$\frac{1}{C_{\mathrm{Hf-SAND}}} = \frac{1}{C_{\mathrm{SiO_2}}} + \frac{1}{C_{\mathrm{HfO}_x\mathrm{priming}}} + n\cdot\left(\frac{1}{C_{\mathrm{PAE}}} + \frac{1}{C_{\mathrm{HfO}_x\mathrm{interlayer}}}\right) \quad (1)$$

Note that although this analysis extends to a total of four multilayers, the present fabrication procedure is not limited to four layers, and additional 2.3 nm thick PAE/HfO_x bilayers can

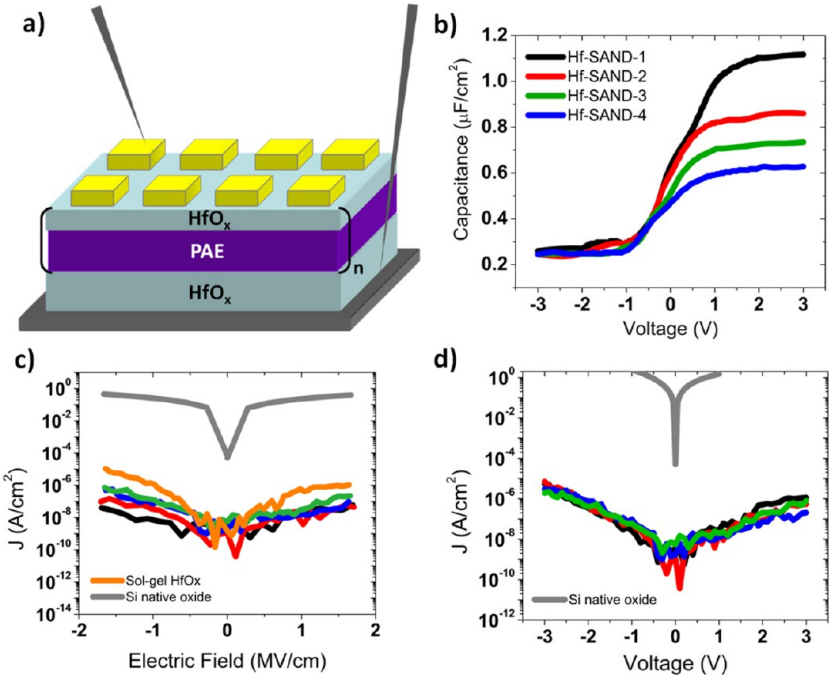

Figure 8. (a) MIS structure scheme for Hf-SAND-*n* dielectrics. (b) 10 kHz Capacitance versus gate voltage data for Hf-SAND-1−4 films. (c) Leakage current density versus electric field (J versus E) and (d) leakage current density versus voltage (J versus V) for Hf-SAND-1−4 films.

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easily be grown to achieve a wide range of desired Hf-SAND thicknesses.

From Table 1 and Figure 8 the Hf-SAND dielectric leakage is several orders of magnitude lower than that of native SiO_2

Table 1. Physical and Dielectric Properties of Hf-SAND-*n* Multilayers

Hf-SAND layers	thickness[a] (nm)	RMS ω[b] (Å)	J[c] (A/cm^2)	C_i[d] (μF/cm^2)	k_{eff}	EOT[e] (nm)
1	6.5	1.3	3.9×10^{-8}	1.10	8.1	3.1
2	8.8*	1.4	9.7×10^{-8}	0.850	8.5	4.1
3	11.0*	1.5	4.9×10^{-7}	0.720	9.0	4.8
4	13.3	1.7	7.2×10^{-7}	0.610	9.2	5.7

[a]XRR-derived. The bilayer and trilayer thicknesses are interpolated values from the XRR derived PAE/HfOx bilayer thicknesses and further verified by the expected inverse decrease in capacitance and increases in effective dielectric constant. [b]Determined by AFM. [c]Measured at −2 MV/cm. [d]Measured at 10 kHz. [e]SiO_2 EOT.

capacitors (1 A/cm^2 at ±2 MV/cm) and is comparable to previous reports utilizing either solution phase self-assembly[15a] or vacuum deposition dielectric growth techniques, such as ALD,[36] which typically afford optimized leakage current densities of ~10^{-8} A/cm^2 or less. At the extremes of the bias window, the present Hf-SAND current leakage densities of 10^{-6} A/cm^2 translate to only a few hundreds of pA leakage current in conventional TFT structures. In fact, single-layer 4.7 nm Hf-SAND films exhibit a resistance to leakage that is 2 orders of magnitude greater than similarly fabricated 18 nm thick single-layer sol−gel HfO_x dielectric capacitors when normalized to the same applied electric field (Figure 8c). The thicker, multilayer Hf-SAND variants exhibit significantly lower electric field normalized leakages which should allow larger voltage biasing windows, useful for a number of transistor applications. Breakdown studies of the films (Figures S6, S7, Table S1) indicate that the Hf-SAND multilayers are resilient to large applied electric fields, with average breakdown fields (E_{BD}) of ~5.5 MV/cm (Figure S6). This is similar to the Zr-SAND and silane-based SANDs which typically exhibit breakdown resistance up to E_{BD} ~ 6 MV/cm (see Table S1).[37,15i] Note that the 250 °C annealing of a four-layer Hf-SAND increases the breakdown strength of the films even further, to nearly 8 MV/cm (Figure S7), which is near the upper range of all previously reported SAND dielectrics.[37,15i] Furthermore, taking into consideration the relatively large 150 × 150 μm Au contact pad area used here to probe the leakage and capacitance in these structures, it can be concluded that the Hf-SAND self-assembly process affords very high quality, nearly pinhole-free dielectric films.

To better assess the performance enhancements afforded by introducing HfO_x nanolayers into SAND structures, the dielectric properties of structurally similar SAND type II[15i] and Zr-SAND[15a] structures (Figure 2) are next compared with Hf-SAND. Note that the newly developed Hf-SAND system compares favorably with previous SANDs in terms of minimal leakage current but offers significantly increased capacitance, reduced surface roughness, and other desirable dielectric-based attributes. Thus, a single layer of Hf-SAND can achieve a capacitance density greater than 1 μF/cm^2 (1.1 μF/cm^2 measured) versus 0.75 μF/cm^2 for a single layer of Zr-SAND, and 0.71 μF/cm^2 for the silane-based SAND type II structure reported in the literature.[15a,i] This represents a capacitance enhancement of nearly 50% over current-generation SAND materials and enables microfarad capacitance densities for the first time from a solid-state SAM-metal oxide hybrid dielectric which is processable at low temperatures in ambient. In addition, the large increase in effective dielectric constant (k_{eff}) of the Hf-SAND system (Table 2) in conjunction with a comparable or greater breakdown strength (E_{BD}) versus Zr-SAND (~6−8 MV/cm) enables a very significant increase (~35%) in the theoretical maximum dielectric displacement field ($D_{MAX} = \varepsilon_0 k_{eff} E_{BD}$)[38,37a] attainable when using Hf-SAND over that of earlier SAND variants. Dielectric displacement fields of up to 3.9 μC/cm^2 (see Table S1) are possible at the single-layer limit (Hf-SAND-1), which nears the performance benchmarks of current state-of-art oxide gate dielectrics grown by ALD.[38] By this metric it can be seen that critical dielectric properties (leakage, breakdown resistance) with Hf-SAND are not compromised with the large capacitance enhancement.

An alternative metric of dielectric performance is effective oxide thickness (EOT) in nanometers of SiO_2, which for the entire dielectric stack (including the 1.8 nm native oxide) is reduced by a minimum of 33% in Hf-SAND (down to 3.1 nm) versus both type II SAND and Zr-SAND. Note also that the effective permittivity can be extracted for the (HfO_x-PAE-HfO_x) trilayer structure, which is increased significantly from k_{eff} = 5.5 in Zr-SAND, to k_{eff} = 8.1 in Hf-SAND. This demonstrates improved dielectric performance afforded by both the HfO_x and the π-electron PAE layers over that of Zr-SAND construction. Many of these properties are summarized in Table 2.

Figure 9 graphically illustrates Hf-SAND dielectric trends in terms of capacitance density versus the bilayer n number, inverse capacitance versus n, EOT, and overall dielectric permittivity (k) of Hf-SAND versus thickness. Note also that as n increases, the overall dielectric constant (k_{eff}) also increases. This implies that the PAE layer, which is the majority component in subsequent layers, has a larger k than that of the inorganic oxide. This supports the conclusion of Yoon et al.[15i] that the stilbazolium group has very high permittivity; generally greater than what can normally be achieved with low temperature sol−gel oxides. Thus, the SAND architectural concept can be viewed as an overall more promising approach

Table 2. Comparison of Hf-SAND-1 Dielectric Properties with those of Structurally Analogous Dielectrics Reported Previously[15a,i]

nanodielectric type (stacking motif)	thickness[a] (nm)	RMS ω[b] (nm)	J[c] (A/cm^2)	C_i[d] (μF/cm^2)	k_{eff}	EOT[e] (nm)	k organic π-layer	k oxide layer
SAND type II[15i] (Stb-SiO_x)	3.2	<1.0	6×10^{-6}	0.710	4.0	4.9	16	3.9
Zr-SAND-1[15a] (ZrO_x-PAE-ZrO_x)	4.7	0.15	9×10^{-8}	0.750	5.5	4.6	7	10
Hf-SAND-1 (HfO_x-PAE-HfO_x)	4.7	0.13	5×10^{-8}	1.10	8.1	3.1	15	13

[a]XRR derived. [b]Determined by AFM. [c]Leakage current density measured at −2 MV/cm. [d]Measured at 10kHz, except for SAND type II which was measured at 100 Hz. [e]SiO_x EOT.

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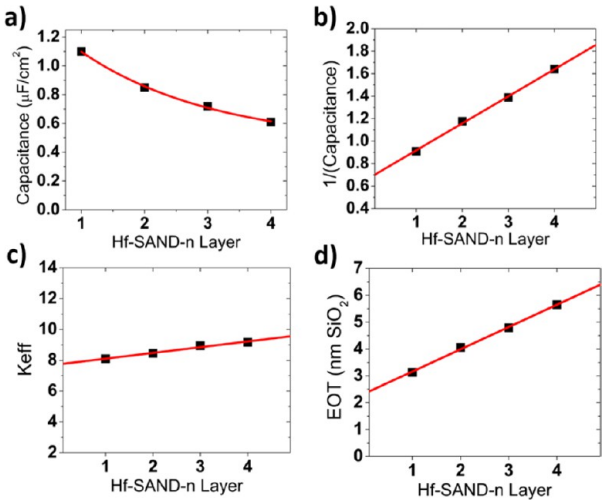

Figure 9. Plots with best fits of Hf-SAND-*n* MIS properties. (a) Assuming $1/x$ decay dependence of capacitance density versus Hf-SAND layer number *n*. (b) Inverse capacitance versus layer number linear relationship. (c) Increasing effective dielectric constant k_{eff} versus layer number *n*. (d) EOT versus layer number *n*.

to high performance gate dielectrics than that offered by sol–gel only or bilayer sol–gel/low-*k* SAM dielectrics.

In regard to the dielectric quality of the present Hf-SAND HfO_x nanolayers, the spectral appearance and relative XPS peak ratios for the O 1s sites in HfO_x (Figure 5) show greater cross-link densities than in ZrO_x sol–gel literature reports for 150 °C process temperatures.[39] Furthermore, the insulating properties of SAND HfO_x layers doubtless benefit from the large amorphous hafnia band gap of 5.7 eV, while that of amorphous zirconia is 1 eV lower, 4.7 eV.[23e] Although increased band gaps typically correlate with lower *k* for most dielectrics,[1a,40] sol–gel processed oxide films seldom attain the maximum theoretical values of *k*, as illustrated by the work of Ha with $k = 10$ for ZrO_x versus $k = 25$ theoretical,[15a] and densification metrics may enhance *k* even in larger band gap materials. Note also that the slightly greater lattice enthalpy and Gibb's free energy of formation for hafnia ($\Delta H_f^\circ = -1145$ KJ/mol, $\Delta G_f^\circ = -1088$ KJ/mol) versus that of zirconia ($\Delta H_f^\circ = -1100$ KJ/mol, $\Delta G_f^\circ = -1042$ KJ/mol) may play a role in promoting the densified oxide matrices achieved at the present low (150 °C) processing temperatures.[41a,23f,41b,c] Such density enhancements are likely to increase the dielectric constant.[42] Furthermore, recent literature suggests that the *k* of HfO_x thin films is far less sensitive to crystallinity or amorphous character than those of ZrO_x,[23b,43] with *k* of the latter varying by 2× or more, depending on polytype (tetragonal or monoclinic).[23b,43] These factors are likely to afford solution-processed hafnia films with more predictable and stable insulating characteristics than those of zirconia.

We can also consider the above XRR results (Figure 6b) to better understand the HfO_x film quality by comparing XRR-derived electron densities of the nanolayers versus those for Zr-SAND obtained in ref 15a. Electron densities for the HfO_x and ZrO_x priming layers, reported relative to the underlying Si substrate, were found to be $2.5\rho_{Si} \pm 0.2$ and $2.1\rho_{Si} \pm 0.3$, respectively (99.7% confidence levels). When compared to the computed values for amorphous HfO_2[44] and ZrO_2[45] ($2.8\rho_{Si}$ and $1.8\rho_{Si}$, respectively), the ZrO_x layers within the Zr-SAND are found to have 0–30% *higher* electron density than expected, while the HfO_x layers within the Hf-SAND are found to have 20–3% *lower* electron density than expected.

There are many potential sources for these differences. For example, the Zr-SAND density may be increased because: (1) the oxide layer stoichiometry may be slightly biased toward Zr; (2) the layers may have a minority (~20%) crystalline phase; or (3) the layers may simply possess a denser than expected amorphous phase. Similarly, there are several possible explanations for the lowered electron density HfO_x layers in Hf-SAND, for example, interlayer mixing, oxygen-biased stoichiometry, or the presence of hydroxyl groups. Additional studies will be needed to fully understand the nature of these differences, however, the overall magnitude of deviation from the expected electron density is rather small for Hf-SAND, supporting the earlier conclusion that the films are generally well cross-linked. The observation of generally lower electron density than in the bulk is also consistent with known behavior of sol–gel processed oxides annealed at relatively low temperatures.[46]

To assess the electronic performance of the present thin-films, HfO_x-only capacitors were also characterized (see SI) and the *k* of HfO_x films extracted identically to that of the 150 °C processed SAND structures. The *k* is found to be ~13; significantly greater than the $k = 10$ reported for analogous sol–gel ZrO_x films.[15a,47] However, as noted earlier, the ~50% increase in capacitance on replacing ZrO_x by HfO_x in SAND structures cannot be explained solely on the basis of oxide *k*'s, and the organic π-layer contribution is discussed next.

Note from Table 2 that the extracted PAE layer *k*-value in Hf-SAND is larger than the corresponding *k* in Zr-SAND. In fact, the Hf-SAND *k* is much closer to that reported for a type II SAND variant by Yoon et al.[15i] Next, XRF was used to quantify the PAE coverage from a Br analysis[48] of similarly fabricated Zr- and Hf-SANDs. The Br surface coverage is found to be 30 ± 10% greater for Hf-SAND than for Zr-SAND (Figure 10; full spectra in Figure S3). Since the permittivity can

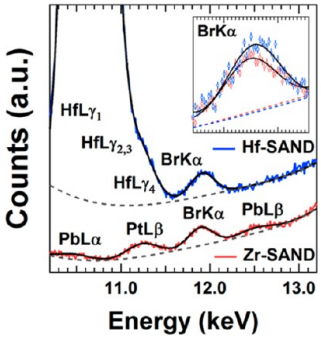

Figure 10. XRF spectra for Zr- (red) and Hf-SAND (blue) with peak-fitting overlays in black and cubic spline background fits in dashed gray. The Br signal (inset) which is associated with the PAE cation is 30% higher for Hf-SAND.

be related to the surface dipole density,[49,42a] the greater PAE density on HfO_x should significantly increase the *k* of this layer. From eq 1 with $k = 13$ for HfO_x, the PAE layer permittivity for single-layer Hf-SAND is estimated to be ~15, which is significantly greater than estimated from eq 1 for single-layer Zr-SAND (Table 2). The origin is reasonably correlated with the ~30% greater PAE coverage extracted by XRF and again is nearly identical to the dielectric permittivity ($k = 16$) reported by Yoon et al. for SAND type II (Table 2).[15i] The greater HfO_x

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surface uniformity evident in the XRR and AFM data may be an additional factor affecting coverage, where slight variations in roughness may interfere with SAM domain ordering and PAE π-stacking.[22,50,23f]

Regarding the aforementioned differences in PAE coverage, note that the comparative surface chemistries of ZrO_x and HfO_x are consistent with these observations. Thus, the isoelectric points ($HfO_2 \approx 8.0$; $ZrO_2 \approx 5.0$)[22,51a−j] and other surface chemical properties[23c,e,29a,50,52a−r] argue that the former oxide is more basic, while chemisorption studies indicate that the binding strength of phosphonic and other carboxylic acids to oxide surfaces generally scales with surface basicity.[15e,22,23c,51d,53a−c] In regard to the final phosphonate binding structure, this has been much discussed, and it is likely that surface-acid hydrogen-bonded species are the precursors of the final condensed covalent ester-like linkages.[19,23c,31a,51d,52c,53c,54a−g] Future work will endeavor to understand additional aspects of the enhanced surface coverage.

This section is concluded by noting that the overall lowest leakage current per applied field obtained to date for a SAND material is for Hf-SAND-1 (Table 2), which offers the concomitant benefits of synthetic expedience and maximum capacitance. Thus, Hf-SAND-*n* films are truly sub-10 nm solution-processed functional dielectric materials. The large breakdown (5.5 MV/cm) and maximum displacement fields D_{MAX} (3.9 μC/cm^2) are promising for the use of Hf-SANDs in electronic devices. Nevertheless, gate dielectric metrics alone are of minimal significance if the materials are incompatible with acceptable/excellent TFT performance. In the next section, we show that high-performance SWCNT TFTs can indeed be fabricated in a straightforward manner on Hf-SAND-1 films via industry standard processing methods, such as photolithography, wet chemical development, direct stamping, high-temperature annealing, long-term solvent exposure, and even oxygen RIE.

Random-Network Carbon Nanotube/Hf-SAND Transistors. In assessing suitable semiconductors to evaluate new gate dielectric materials performance, carbon nanotubes were chosen due to their sensitivity to local environmental factors, such as charged impurities and capacitance.[4a,55] The technological relevance of these materials is a further motivation since SWCNTs offer impressive opportunities in next-generation electronics and optoelectronics, including for sub-10 nm scaling of traditional MOS field-effect transistors.[55c,56] Due to challenges associated with assembling or patterning single nanotubes, thin SWCNT random networks are used here as TFT channels.[57] However, note that random networks may: (1) contain metallic nanotube contaminants which can significantly reduce I_{ON}:I_{OFF} or short the device between the source and drain electrodes; (2) suffer self-screening by the underlying tubes in cases of thick random networks and cannot be turned off due to ineffective capacitive coupling; and (3) suffer tube-to-tube contact resistance in the channel which degrades the carrier mobility, thereby degrading TFT response. For these reasons, an attractive approach to enhance random-network SWCNT TFT performance would be to maximize capacitive coupling of the channel SWCNTs to the gate via high-capacitance dielectric materials.

In the present approach, common back gate, bottom contact devices were fabricated by lithographically patterning Cr/Au contacts directly on the Hf-SAND followed by stamping of vacuum filtered semiconductor enriched SWCNTs onto the device electrodes and channels (Figure 11). After additional

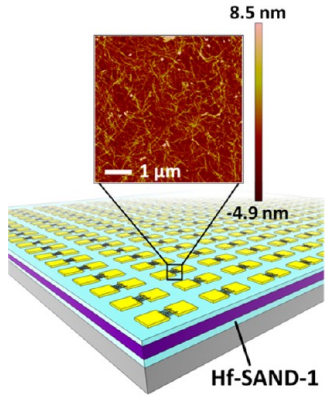

Figure 11. Bottom-contact SWCNT/Hf-SAND-1 TFT geometry with an AFM image of the SWCNT density in the TFT channel.

photolithography and RIE to isolate the devices, the TFTs are ready for electrical measurements. Note that Hf-SAND can withstand annealing temperatures under ambient up to 400 °C (SI) for periods of 15−30 min, which is useful for conventional semiconductor annealing protocols or for removing extraneous SWCNT surfactants, although this was not necessary here. Impressive SAND temperature stability was also noted in previous work with other SAND classes.[15a,58] The present fabrication procedure produces SWCNT random network TFTs between the source-drain electrodes as depicted in Figure 11. Note that both small (150 μm) and large (4660 μm) channel width devices (with various channel lengths from 10 to 100 μm) were characterized, with representative devices depicted in Figures 12 and 13. The TFTs were characterized under ambient conditions with a three-point probe station and shielded from light. The common back gate was accessed directly through the Si with a W probe to ensure good contact, and source-drain electrodes were probed with Signatone SE-SM "cat-whisker" style probes.

The results show that Hf-SAND-1 offers an exceptionally high capacitance density of 1.1 μF/cm^2 when measured in the accumulation regime of the silicon back-gate substrate (Figure 8b). In the common back gate, bottom contact geometry, the field-effect mobility can then be extracted from eq 2:

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_g V_d} \tag{2}$$

where L_{ch} is the channel length, W_{ch} is the channel width, and g_m is the transconductance, given in eq 3, which is the slope of the linear−linear plot of the drain current versus gate voltage (I_d−V_g) at a constant source-drain bias. In the general case of TFTs with continuous films

$$g_m = \frac{\partial I_d}{\partial V_g} \tag{3}$$

of organic or inorganic semiconductors, the field-effect mobility can be calculated straightforwardly from the channel capacitance C_g assuming a parallel plate geometry as in eq 4, where t_g is the overall thickness of the gate dielectric (6.5 nm for Hf-SAND-1 inclusive of native SiO_2), k is the effective dielectric constant (8.1 for Hf-SAND-1), and $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m is the permittivity of free space. The parallel-plate field-effect mobility is then calculated using $C_g = C_{PP} = 1.1$ μF/cm^2.

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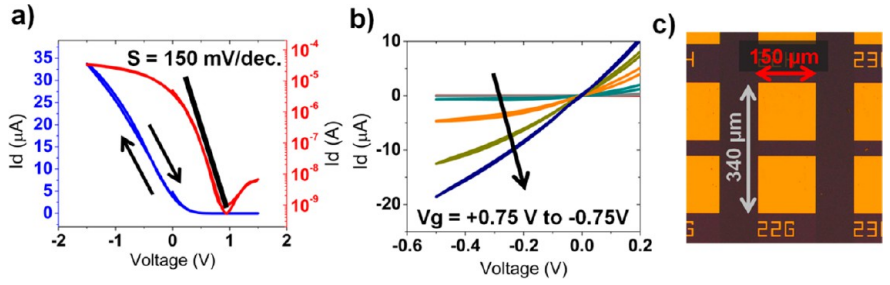

Figure 12. (a) SWCNT/Hf-SAND-1 TFT log–linear and linear–linear transfer plots indicating low I–V hysteresis, V_d = 500 mV, L = 40 μm, W = 100 μm. Red = source-drain current on log–linear scale, and blue = source-drain current on linear–linear scale. (b) SWCNT Hf-SAND-1 TFT output plot. (c) Plan view of the corresponding device structure. Dimensions are in μm.

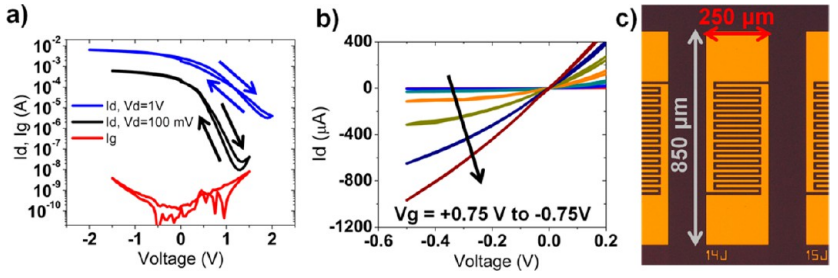

Figure 13. (a) Large area SWCNT/Hf-SAND-1 TFT transfer plot with concurrently measured dielectric leakage, V_d = 100 mV (black), 1 V (blue), L = 10 μm, W = 4660 μm. (b) SWCNT Hf-SAND-1 TFT output plot indicating large drive currents. (c) Plan view of the corresponding device structure. Dimensions are noted in μm.

Table 3. SWCNT TFT Geometry and Response Parameters for Hf-SAND-1 Based Devices[a]

device	C_{PP} / C_{in} (μF/cm^2)	μ_{PP} (cm^2/(V s))	μ_i (cm^2/(V s))	I_{ON}:I_{OFF}	V_{th} (mV)	channel geometry ($L \times W$, μm)
1	1.1/0.166	20	130	8.0 × 10^4	~200	linear (40 × 100)
2	1.1/0.166	21	137	6.5 × 10^4	~350	linear (100 × 150)
3	1.1/0.166	17	110	8.0 × 10^4	~500	serpentine interdigitated (10 × 4660)

[a] V_d = 500 mV (device 1), 100 mV (device 2), and 100 mV (device 3).

$$C_g = C_{PP} = \frac{\kappa\varepsilon_0}{t_g} \quad (4)$$

Caution must be exercised, however, when modeling CNT networks as continuous films since such networks may be randomly distributed across the transistor channel with voids that can lead to overestimation of the gate-nanotube capacitive coupling.[59,5b] Thus, using C_{PP} in the mobility expression (eq 2) significantly overestimates the capacitance applied to the CNT films at low nanotube network densities (generally assumed when <100 SWCNTs/μm are present) and thus offers a lower bound on the actual mobility. From AFM our linear density is estimated to be 15 SWCNTs/μm, which is well below this density limit. The present TFTs exhibit exclusively p-channel behavior which is expected for unencapsulated SWCNTs operated under ambient. A summary of device performance is given in Table 3. Utilizing eqs 2–4, the extracted parallel plate mobilities (μ_{PP}) are ~20 cm^2/(V s), which are in accord with literature reports for random nanotube networks.[60] Note that some previous literature reports have included quantum capacitance correction factors, which reduce the calculated channel capacitance and result in derived mobilities likely near the upper bounds.[61] Therefore, initial analysis here indicates that the present lower bound mobilities are comparable to previous upper bound reports, indicating very high intrinsic device performance. Not only does this result demonstrate the favorable performance characteristics of the Hf-SAND dielectric material, but it exemplifies the need for standardized reporting of SWCNT device performance metrics, including quantum capacitance corrections when reporting intrinsic device performance in high-capacitance systems. Therefore, to extract the intrinsic mobility, the quantum capacitance correction model is employed next, and the calculated intrinsic capacitance (C_{in}) is included in place of the parallel plate capacitance since this accounts for the electrostatic coupling between the CNTs (as a reflection of SWCNT network density) as well as the SWCNT quantum capacitance.

If the intrinsic capacitance is defined as C_{in}, and the quantum capacitance C_Q, which is known for SWCNTs, is inserted, then C_{in} can be extracted from the linear density of SWCNTs in the channel (Λ_0^{-1}) according to eq 5, where Λ_0^{-1} is the linear density of SWCNTs (SWCNTs/μm), $C_Q = 4.0 \times 10^{-10}$ F/m is the quantum capacitance of SWCNTs,[62] R is the radius of SWCNTs (0.72 nm for arc-discharge SWCNTs), and k is the dielectric constant of the entire dielectric stack.

$$C_g = C_{in} = \left\{ C_Q^{-1} + \frac{1}{2\pi\kappa\varepsilon_0} \ln\left[\frac{\Lambda_0}{R\pi} \sinh\left(\frac{2\pi t_g}{\Lambda_0} \right) \right] \right\}^{-1} \Lambda_0^{-1} \quad (5)$$

We have extracted a linear density (Λ_0^{-1}) in the TFT channel of 15 SWCNTs/μm from the AFM data (Figure 11) as mentioned briefly above, which is near the ideal density recently reported by Sangwan, et al.[57b] The parallel plate

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capacitance, quantum capacitance correction, and lower and upper bound mobilities are summarized in Table 3. While in the case of the parallel plate model, the field-effect mobilities are modeled as reported earlier, when the quantum capacitance is considered, the intrinsic mobilities (μ_{in}) emerge very near to the highest reported to date for a random network (RN) CNT transistor (~130 cm^2/V s).[57b,60d,63a−c,60e,63d−f,14,35] This demonstrates the utility of combining high capacitance SANDs with DGU sorted SWCNTs for future technological applications.

Very steep subthreshold swings of 150 mV/dec (Figure 12), which also rival the smallest reported to date for RN-CNT TFTs, indicate low levels of interface trapped charge.[57b,60d,e,64,14,35] The well-behaved threshold voltage (SI) and overall low operating voltages in conjunction with the outstanding subthreshold swing indicate excellent capacitive coupling of the SWCNT thin films and renders these devices potentially useful for ultralow-power device applications. Large-area TFTs were also fabricated to exploit the conformal and defect-free nature of Hf-SANDs and to assess the magnitude of the transconductances that can be achieved (Figure 13). Note that one of the more remarkable aspects of Hf-SANDs is the ability to produce relatively large area devices (as shown in Figure 13) on top of a sub-10 nm solution processed film. It can be seen that TFTs on the order of ~0.2 mm^2 in dimension exhibit stable performance and low leakage on top of the only 6.5 nm thick Hf-SAND-1 film. Milliamp output currents are achievable at sub-1 V bias enabling record >5 mS transconductance with I_{ON}:I_{OFF} = 10^5 and a leakage (I_g) of a few nanoamps. This is the first time that such large transconductance parameters have been reported without a fall in the SWCNT device I_{ON}:I_{OFF} (Figure 14). This is undoubtedly related to the ability of Hf-SAND to capacitively couple large populations (>700 000) of SWCNTs within device geometries.

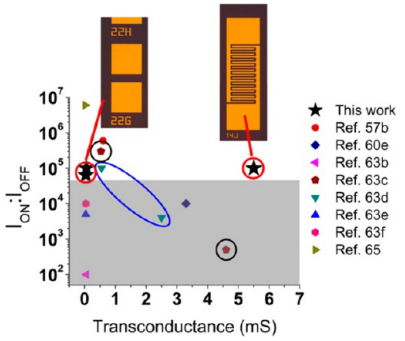

Figure 14. Plot of TFT transconductance versus I_{ON}:I_{OFF} from recent literature and from the present work (black stars, red circles). The blue and black circled points are related systems where device parameters, such as SWCNT network density, device channel dimensions, or SWCNT purity, were varied. Gray shaded area represents low I_{ON}:I_{OFF} region generally unsuitable for digital electronics.

Two recent ground-breaking publications (black and blue circles, Figure 14)[63c,d] report high TFT performance at low SWCNT coverages and/or small device dimensions, which reduces the overall transconductance. At higher SWCNT densities, the I_{ON}:I_{OFF} decreases significantly and typically to the point of unsuitability for digital electronics applications which is depicted graphically in Figure 14 by the higher transconductance points dropping into the gray-shaded region. While normalized transconductance (via the channel width) may be high in these devices, the overall current and transconductance achieved by the present Hf-SAND devices should be important for high-power amplifier or logic applications, where the large intrinsic performance would enable unprecedented device output powers, possibly approaching 20 mW. The present Hf-SAND TFTs achieve this record transconductance performance without falling below the digital electronics threshold (Figure 14) as mentioned above, which is promising for future efforts with SWCNTs in electronics.

CONCLUSIONS

A structurally regular, chemically/thermally robust, all-solution processed at low temperature hafnia-organic self-assembled nanodielectric (Hf-SAND) with impressive dielectric performance is demonstrated. This new dielectric exhibits very low surface roughness, a regular superlattice structure of alternating HfO_x and PAE organic π-layers and an exceptionally large capacitance—2× greater than the previously developed SAND dielectric materials. To illustrate the utility of this Hf-SAND, random network sorted SWCNT TFTs are fabricated on single-layer Hf-SAND and achieve record transconductance while rivaling other state-of-the-art parameters, including mobility and subthreshold swing metrics.[60a,57b,60b−e,65] The present gate dielectric is robust to conventional lithographic processing and fabrication steps as evidenced by the low leakage currents in SWCNT TFTs. The characterization data indicate that the enhanced Hf-SAND capacitance is related to the relatively large metal oxide dielectric constant and increased PAE chemisorption, as argued by the greater surface coverage. This is the first report where phosphonic acid surface binding selectivity affords a dramatic change in device electrical properties, which is undoubtedly valuable for future hybrid organic−inorganic device design protocols. Thus, Hf-SAND should be suitable for a range of applications, including low-cost, low-temperature fabrication, transparent and mechanically flexible electronics, both organic and inorganic, and high-performance carbon nanomaterial electronics and optoelectronics. Furthermore, this hybrid dielectric processing technique offers a potential path to other new classes of hybrid organic−inorganic materials having superlattice structures in which both the organic and inorganic components can be varied.

ASSOCIATED CONTENT

Supporting Information

XRF spectra, TFT threshold voltage, sol−gel only capacitor data, high-temperature annealing data, electrical breakdown data, detailed experimental protocols, and additional cross-section TEM images. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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