Charge Trapping States at the SiO_2—Oligothiophene Monolayer Interface in Field Effect Transistors Studied by Kelvin Probe Force Microscopy

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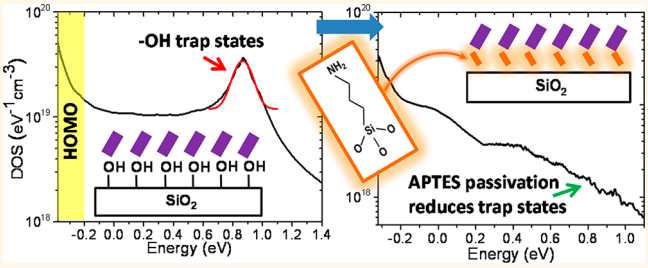
ABSTRACT Using Kelvin probe force microscopy (KPFM) we studied the local charge trapping states at the SiO_2—oligothiophene interface in a field effect transistor (FET), where SiO_2 is the gate dielectric. KPFM reveals surface potential inhomogeneities within the oligothiophene monolayer, which correlate with its structure. A large peak of trap states with energies in the oligothiophene's band gap due to hydroxyl groups is present at the oxide surface. We show that these states are successfully eliminated by preadsorption of a layer of (3-aminopropyl)triethoxysilane (APTES). Time-resolved surface potential transient measurements further show that the charge carrier injection in the nonpassivated FET contains two exponential transients, due to the charge trapping on the oxide surface and in the bulk oxide, while the APTES-passivated FET has only a single-exponential transient due to the bulk oxide. The results demonstrate that APTES is a good SiO_2 surface passivation layer to reduce trap states while maintaining a hydrophilic surface, pointing out the importance of dielectric surface passivation to bridge the gap between soft materials and electronic devices.



KEYWORDS: charge trapping · oligothiophene monolayer · field effect transistor · Kelvin probe force microscopy · density of states

Organic electronics is an emerging area both for fundamental research and industrial applications.[1−4] Compared to their inorganic counterparts, organic semiconductors are often low cost, solution processable, and environmentally friendly, with applications in large-area electronics including field effect transistors (FETs), solar cells, light-emitting diodes, and radio frequency identification tags.[1−7] More recently, organic semiconductors have found applications in biosensors and bioelectronics.[8,9]

The bottleneck in the performance of most organic electronic devices is the relatively low charge carrier mobility, due to both the intrinsic charge carrier localization and hopping transport mechanism, and various defect-induced charge trapping effects.[1−3,10−14] For FETs, the dielectric—organic semiconductor interface is crucial since the charge carriers are within a few nanometers of this interface. Unfortunately, one of the most widely used dielectrics, SiO_2, is notorious for electron trapping, possibly due to bulk defects and surface hydroxyl groups.[10,11] To reduce this charge trapping effect, various siloxane self-assembled monolayers (SAMs) (*e.g.*, hexamethyldisilazane (HMDS) and octadecyltrichorosilane (OTS)) have been used to passivate the SiO_2 surface.[10−14] This approach, though effective in alleviating charge trapping and increasing conductivity, always results in a hydrophobic surface, which is not compatible with some self-assembly (*e.g.*, Langmuir—Blodgett (LB) deposition) and biosensing techniques.[15]

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To quantitatively characterize charge trapping effects and understand the trapping mechanism, the density of electronic states (DOS), which reveals the charge carrier's energy dispersion, is fundamentally important. The localized trap states are often in the HOMO−LUMO gap of the organic semiconductors, which has been measured by various techniques including ultraviolet photoelectron spectroscopy,[16] transient photovoltage spectroscopy,[17] and Kelvin probe force microscopy (KPFM).[18] Among these techniques, KPFM allows for a quantitative direct determination of DOS with spatial resolution down to 20 nm. Moreover, it is suitable for measuring the DOS of the organic semiconductor channel on top of the dielectric surface on an FET, which is directly relevant to device performance.

Here we present results obtained using KPFM to study the charge trapping behavior of an oligothiophene monolayer FET. The schematic setup of the measurement is shown in Figure 1a,b, where the only difference between parts b and a is the preadsorption of an APTES self-assembled monolayer on the SiO_2. The FET channel is a submonolayer of an oligothiophene derivative, named 4-(5-decyl-2,2′;5′,2″;5″,2‴;5‴,2⁗-pentathiophen-5-yl)butyric acid (Figure 1c), abbreviated D5TBA.[19−22] This molecule has a semiconducting core consisting of five thiophene rings, which is widely used for molecular electronics.[23−25] Moreover, it is amphiphilic with a hydrophilic carboxylic acid group at one end and a hydrophobic alkyl chain at the other end, and thus is a good model system for self-assembly at the air−water interface. KPFM reveals spatial inhomogeneity of the D5TBA surface potential distribution, which correlates with the structure of the monolayer film. Our spectroscopic measurements show that the HOMO edge level of the D5TBA is 0.2 eV below the Au Fermi level and that the D5TBA FET is p-type, in agreement with previous conductive AFM measurements in our group.[19,22] For the nonpassivated FET, we observe mid-gap trap states with a Gaussian peak at 1.07 eV above the HOMO edge present at the D5TBA−SiO_2 interface. After APTES passivation, these states are greatly reduced, resulting in an exponentially decaying DOS in the band gap. Furthermore, we performed time-resolved local surface potential measurements on D5TBA crystalline domains on top of the nonpassivated and APTES-passivated FET, revealing that the nonpassivated FET has a larger hysteresis. To the best of our knowledge, this is the first report on SiO_2 surface passivation with hydrophilic SAM that successfully reduces charge traps. These results could be interesting for the interdisciplinary areas of soft materials and electronics, such as self-assembled organic electronics and bioelectronic interfaces.

RESULTS AND DISCUSSION

The FET substrate was fabricated using a standard photolithography process, with a thermal oxide

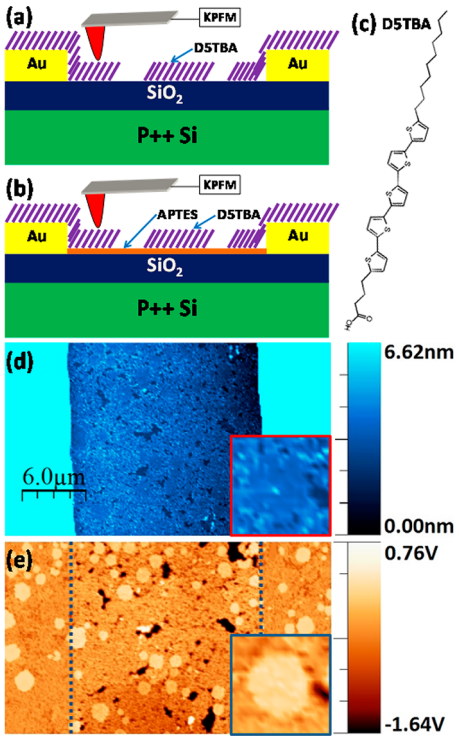

Figure 1. Schematic setup of the KPFM measurement, with the tip above a D5TBA monolayer domain on a FET (a) without oxide surface passivation and (b) with APTES passivation. (c) Molecular structure of 4-(5-decyl-2,2′;5′,2″;5″,2‴;5‴,2⁗-pentathiophen-5-yl)butyric acid (D5TBA). Simultaneous (d) topography and (e) surface potential images of a nonpassivated D5TBA FET. The gate bias is −13 V. The blue dotted lines in (e) mark the position of the Au−SiO_2 interface. Note that the Au electrodes in (d) (cyan colored) are actually 50 nm above the oxide in the middle with the height color scale saturated, while in (e) the crystalline domains of the D5TBA monolayer are clearly distinguishable both on Au and on oxide. The insets in the bottom right corners of (d) and (e) are expanded images of one area on the oxide.

thickness t_{ox} = 300 nm, channel length L = 20 μm, and width W = 1 mm. The D5TBA monolayers deposited from the Langmuir−Blodgett trough attach to both the oxide and the Au surface *via* the carboxylic acid end group, while the C10 alkyl chain stays on top, rendering the surface completely hydrophobic (as confirmed by water contact angle measurements). The D5TBA FET was stored in an Ar glovebox for at least 24 h before KPFM measurements, so as to remove most of the water. KPFM was performed using an Agilent 5500 AFM with a home-built Kelvin probe setup. In order to achieve high spatial and energetic resolution, we implemented the single pass frequency modulation method for the Kelvin probe feedback loop[26] (see Methods section for details). With this setup we can measure the surface potential V_{sf} with 20 nm spatial resolution and 20 mV potential resolution. The KPFM measurements were performed at room temperature in a nitrogen chamber with relative humidity of <0.5% (the detection limit of our hygrometer). During the surface potential measurements the Au

source and drain electrodes (shown in Figure 1a,b) were grounded, while the gate bias V_g was varied within the range of −100 to 100 V. It should be noted that we operated the FET in the static field effect capacitor regime, since no source−drain bias was applied. Assuming that the channel potential is uniform across the vertical cross section of the FET channel, and the thermal broadening of the Fermi−Dirac distribution at room temperature is negligible compared to the energy scale of the measurement,[27,28] we can use a simple parallel plate capacitor model to extract the carrier density in the channel:

$$N = \frac{C_{ox}}{t_c q}[(V_g - V_t) - V_{sf})] \quad (1)$$

where C_{ox} is the oxide capacitance per unit area, t_c is the channel thickness, q is the elementary charge, and V_t is the threshold gate voltage for charge carrier injection into the channel (the origin of the x-axis in Figure 3a,d). We can write the energy level of the channel as the difference between the vacuum level and Fermi level, which is simply

$$E = qV_{sf} \quad (2)$$

The DOS can be obtained as

$$\frac{dN}{dE} = \frac{C_{ox}}{t_c q^2}\left(\frac{1}{\frac{dV_{sf}}{dV_g}} - 1\right) \quad (3)$$

It should be noted that the D5TBA monolayer channel in our FETs is only 1.5 nm thick, as determined by AFM measurements. This ultrathin monolayer channel ensures minimum band bending in the vertical cross section of the channel, allowing the technique to reach its limit in terms of the accuracy and range of the extracted DOS.[27,28]

Figure 1d,e show the simultaneous topography and surface potential images of the nonpassivated D5TBA submonolayer FET, with a gate bias of −13 V. The Au source/drain electrodes are 50 nm thick, and the contrast of the topography image is adjusted to show the D5TBA monolayer structure on oxide. Note that the color scale is saturated over the electrodes. Since the surface of the oxide has a roughness of about half a nanometer, the topography of the D5TBA on the oxide, though resolvable, is not very clear. On the other hand, the surface potential image clearly resolves different structures of the D5TBA monolayer film on both Au electrodes and the oxide surface. The D5TBA forms both crystalline domains (brighter, smooth islands) and amorphous domains, consistent with previous studies in our group.[22] Expanded topographic and surface potential images of an island on the SiO_2 are shown in the insets of Figure 1d,e. A detailed analysis of more than 20 surface potential images on different areas and different samples shows that the D5TBA monolayer always has a higher surface potential (lower work function) than the substrate. This is due to the fact that the negatively charged carboxylic end of the D5TBA is down in contact with the surface, while the positively charged alkyl chain end is on top. On the Au electrodes, the average surface potential of the crystalline domains is 250 mV above that of Au, while the amorphous domains have an average surface potential 200 mV above that of Au. We suspect that the amorphous domains could be less densely packed than the crystalline domains, resulting in a smaller electric dipole moment. This could also be an explanation for the fact that no lateral charge transport through the amorphous domains has been observed by previous conductive AFM studies in our group.[19,22] In this study we focus on the crystalline domains.

To understand the surface potential contrast shown in Figure 1e, we zoom in on the Au−SiO_2 interface to analyze the correlation between topographic structure and surface potential, and the dependence of surface potential distribution on gate bias. Figure 2 shows the simultaneous topography (Figure 2a,c) and surface potential (Figure 2b,d) measurements with negative and positive gate biases, respectively. In Figure 2b we can see that there is a D5TBA monolayer island straddling the Au and the SiO_2. When $V_g = -13$ V, the surface potential of the D5TBA on SiO_2 is only slightly (100 mV) below the surface potential of D5TBA on the Au electrode (Figure 2b). But when $V_g = 6$ V, the surface potential of the D5TBA on SiO_2 is 1.1 V above that of the D5TBA on Au (Figure 2d). This indicates that, with negative gate bias, hole carriers can be injected into the D5TBA channel (*i.e.*, the part of the D5TBA island on SiO_2 in electrical contact with the Au). The injected hole carriers effectively screen the gate bias, so that the surface potential of the channel remains close to the surface potential of the source/drain electrodes. When positive gate bias is applied, the hole carriers in the channel are depleted while no electrons are injected, so that the channel becomes insulating and follows the gate bias. These results lead to the conclusion that the D5TBA FET is p-type. Note that the surface potential is noisy within about 100 nm of the SiO_2−Au interface, due to a sharp transition of the topography, which perturbs the feedback loop of the KPFM, when the AFM tip scans across the interface.[26] But the KPFM feedback is stable farther away from the interface. Also, the topography images in Figure 2a and c are identical, indicating that the KPFM technique successfully eliminates the contribution of electrostatic tip−sample interaction to the topography defects, which exists for normal tapping mode and noncontact AFMs without Kelvin probe feedback.[29−31] Moreover, as indicated before, we can see that the surface potential of the D5TBA crystalline island on Au is 250 mV above that of the Au, in both Figure 2b and d.

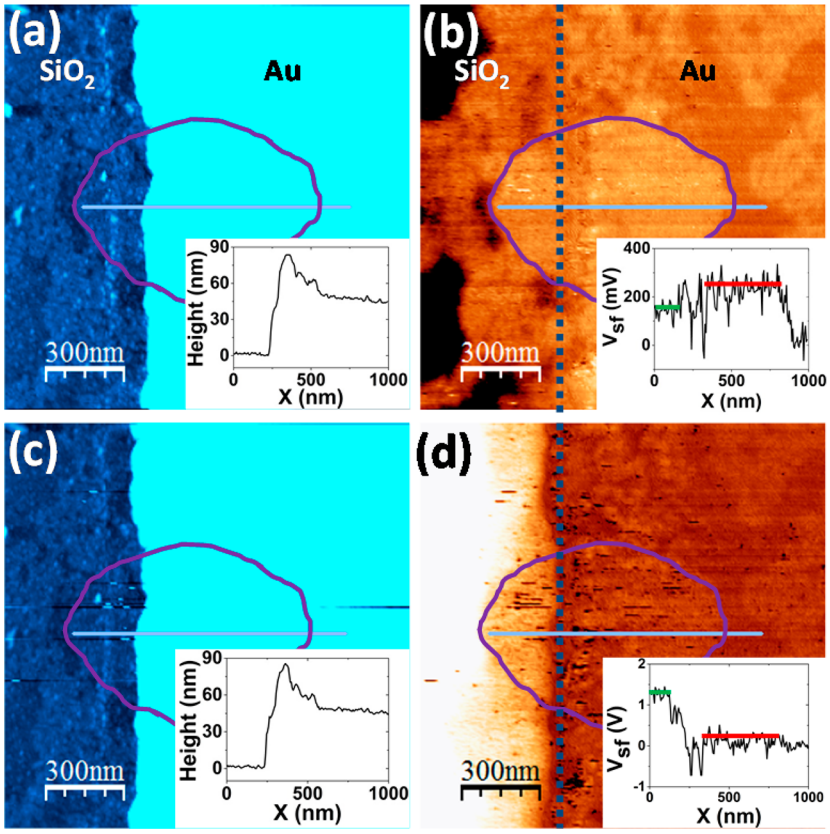

Figure 2. Simultaneous topography (left) and surface potential images (right) of nonpassivated D5TBA FET. The top images correspond to a gate voltage of $V_g = -13$ V, while the bottom images correspond to $V_g = 6$ V. The crystalline monolayer island across the oxide−Au interface is outlined in all the images. The insets show the height and surface potential distributions across the line on this island. The green and red lines in the inset images mark the surface potential level of the D5TBA on SiO_2 and D5TBA on Au, respectively. The blue dotted lines in (b) and (d) show the SiO_2−Au interface, as guidance to the eye.

To quantitatively characterize the dependence of surface potential on gate bias and extract the band gap DOS, we perform $V_{sf}-V_g$ spectroscopy on the crystalline channel region of the nonpassivated D5TBA FET, as shown in Figure 3a. After acquiring each $V_{sf}-V_g$ spectrum the gate bias was set to 0 V for a few minutes to allow the threshold voltage to equilibrate, before taking the next spectrum or image. During the gate bias sweep (at a speed of 10−20 mV/s for all the $V_{sf}-V_g$ spectroscopy measurements), the tip is within 10 nm above the point at the D5TBA island on the oxide, marked by the cross in the inset of Figure 3a. It can be seen that the surface potential linearly follows the gate bias when $V_g - V_t > 0$, confirming that the D5TBA is not electron-conducting. In the linear region the slope is 0.6, a value less than 1 due possibly to charge trapping hysteresis. When $V_g - V_t$ is less than 0, the surface potential remains stable until $V_g - V_t$ reaches −18 V, at which point V_{sf} decreases further until reaching a constant value at $V_{sf} = -0.4$ V. This clearly shows that the hole carriers are injected into the channel, which screen the gate bias. Using eq 3 we can extract the DOS, as plotted in Figure 3b. We can see that the valence band edge DOS is exponential (DOS $\propto \exp(-E/E_0)$) with a characteristic energy E_0 = 0.12 eV, in agreement with previous studies of organic FETs.[18,27] However, the DOS does not decay exponentially all the way into the band gap region. Instead, we observe additional DOS with a Gaussian peak centered at 0.87 eV with a DOS of 3.4×10^{19} eV^{-1} cm^{-3} and a fwhm of 0.15 eV. The band gap of D5TBA can be estimated from the UV−vis absorption edge to be 2.5 eV (see Supporting Information, Figure S1). If we take the Au work function to be 5.1 eV, then the HOMO and LUMO edge of the D5TBA are 5.3 and 2.8 eV below vacuum level, respectively. The peak of the mid-gap trap states is very deep, at about 4.2 eV below vacuum level, which is unlikely due to the electrochemically induced impurities in the D5TBA.[32] We suspect that the hydroxyl groups on the SiO_2 surface are the origin of the deep electron traps (Figure 3c).

With the goal of understanding the nature of the mid-gap traps and eliminating them, we deposited a monolayer of APTES on the FET substrate, after which D5TBA was deposited. The ethoxy groups of the APTES react with the hydroxyl groups on the oxide to form covalent −Si−O−Si− bonds (Figure 3f). To confirm the successful deposition of APTES, we deposited APTES on pure SiO_2 and measured the water contact angle to be 62°. Furthermore, with X-ray photoelectron

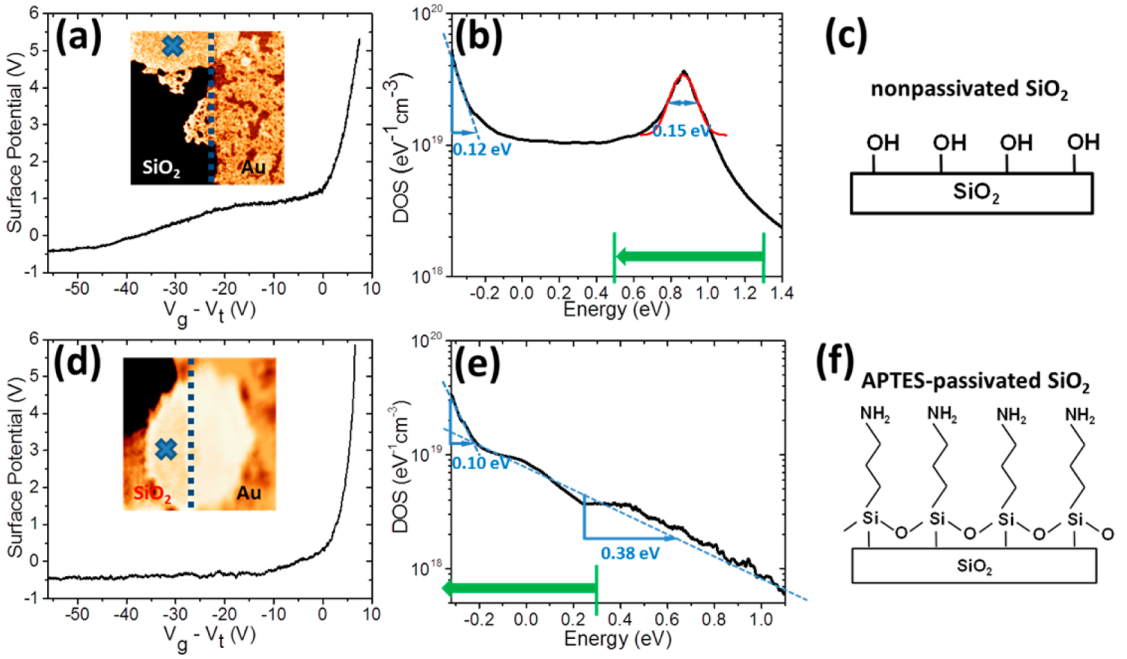

Figure 3. Surface potential−gate bias spectroscopy of a D5TBA FET (a) without oxide surface passivation and (d) with APTES passivation of SiO_2. V_{sf} is calibrated by setting the Au surface potential to zero. The insets in (a) and (d) are 3 μm × 3 μm surface potential images with $V_g - V_t = -13$ V, where the Au−oxide interface is marked with blue dotted lines, and the point at which the V_{sf}−V_g spectroscopy is performed is marked by crosses. The gate bias is swept from positive to negative, with a speed of 10−20 mV/s. (b and e) Corresponding DOS of the D5TBA FET without and with APTES passivation of the SiO_2. (c and f) Schematic surface structure of the SiO_2 before D5TBA deposition. While the nonpassivated SiO_2 surface has OH groups (c), the APTES passivation eliminates the OH groups, leaving a surface terminated with NH_2 groups (f). The red curve in (b) is a Gaussian fit of the DOS peak between 0.64 and 1.10 eV, centered at 0.87 eV with a fwhm of 0.15 eV. The exponentially decaying parts of the DOS in (b) and (e) are marked with dashed lines, with their characteristic energy indicated. The green lines and arrows in (b) and (e) show the start and end positions of the surface energy level (corresponding to $V_g = V_t$ and $V_t - 26$ V, respectively) in the transient surface potential measurements shown in Figure 4b and c, respectively.

spectroscopy (XPS) we found a nitrogen 1 s peak at 400.1 eV (Figure S2). AFM measurements confirm that the surface is smooth with a uniform APTES coverage (Figure S3). The same V_{sf}−V_g spectroscopy is performed on the APTES-passivated D5TBA FET, and the DOS is extracted in the same manner as before. The results are shown in Figure 3d,e. Again the point at which the tip is located is marked by the cross in the inset of Figure 3d. The slope of the V_{sf}−V_g curve in the linear region $V_g - V_t > 0$ is 1.0, indicating negligible hysteresis effect in this case. When $V_g - V_t < 0$, the surface potential decreases slowly until reaching the valence band at $V_{sf} = -0.4$ V. The DOS curve in Figure 3e clearly reveals that the mid-gap DOS peak in the nonpassivated FET is eliminated. With the APTES passivation, the valence band edge DOS contains an exponential short tail up to −0.2 eV with a characteristic energy of 0.10 eV, while the band gap DOS is a long exponential tail with a characteristic energy of 0.38 eV. Since there is an exponential DOS tail with similar characteristic energy from −0.4 to −0.2 eV for both nonpassivated and APTES-passivated FET, we can infer that these states could be attributed to the intrinsic HOMO level broadening due to defects of the D5TBA monolayer or to intermolecular electronic coupling effects. The mid-gap states around 0.9 eV in the Gaussian peak of the nonpassivated FET can be attributed to the −OH groups on the SiO_2 surface, while the 0.38 eV exponential decay of the passivated FET can be attributed to charge trapping in the bulk oxide. This was proposed to be due to proton migration.[33−35]

In addition to the quasi-static DOS measurements with very slow gate bias sweeping, we further performed dynamic transient surface potential measurements. The time constant of our KPFM feedback loop is about 5 ms, which sets the resolution of the time scale for the transient measurements. The schematic of the measurement is shown in Figure 4a. At time zero, the gate bias is suddenly switched from V_t to $V_t - 26$ V. This corresponds to a depletion of electrons in the spectral region from 1.3 to 0.5 eV for the nonpassivated D5TBA FET, which covers the Gaussian trap states, as shown by the green lines and arrows in Figure 3b; while for the APTES-passivated FET, it corresponds to electron depletion from 0.3 to −0.4 eV (which is inside the HOMO band), as shown by the green line and arrow in Figure 3e. Using eq 1, we can estimate that the amounts of depleted electron density (with gate bias sweep from V_t to $V_t - 26$ V) for the nonpassivated and passivated FETs are 2.1×10^{19} and 2.0×10^{19} cm^{-3}, correspondingly, which are very close. The surface potential transients are recorded at the same location

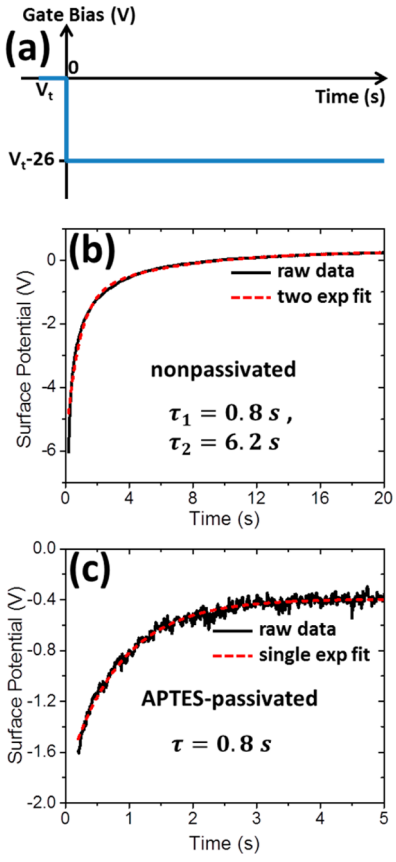

Figure 4. Transient surface potential spectra. (a) Schematic showing the gate bias step function from V_t to $V_t - 26$ V at time 0. For the nonpassivated D5TBA FET, $V_g = V_t$ and $V_t - 26$ V correspond to $V_{sf} = 1.3$ and 0.5 V, respectively, as shown by the green lines in Figure 3b. For the APTES-passivated D5TBA FET, they correspond to $V_{sf} = 0.3$ and -0.4 V, respectively, as shown by the green line and arrow in Figure 3e. The surface potential is recorded from $t = 0.2$ s until it becomes stable, as shown in (b) for nonpassivated FET and (c) for APTES-passivated FET. The black and red-dashed curves are raw data and exponential fits, respectively. While the transient surface potential curve for the APTES-passivated FET can be fitted well with a single-exponential decay with amplitude $A = -1.4$ V and time constant $\tau = 0.8$ s, the transient of the nonpassivated FET requires a fit with a sum of two exponentials, with amplitudes $A_1 = -4.7$ V and $A_2 = -1.5$ V and time constants $\tau_1 = 0.8$ s and $\tau_2 = 6.2$ s.

as marked by the crosses in Figure 3a,d. The results for nonpassivated and APTES-passivated FETs are shown in Figure 4b,c. At $t = 0$ s the surface potential is usually saturated to -10 V (the lower limit of our KPFM surface potential measurements), so we choose to start recording the surface potential beginning at $t = 0.2$ s for all the transient measurements. We can see that the initial surface potential at $t = 0.2$ s is around 6 V below the steady-state surface potential for the nonpassivated FET. After APTES passivation, the initial surface potential is about 1 V below the steady-state surface potential, almost 6 times smaller. Moreover, we can see that the surface potential transient of the APTES-passivated FET fits well with a single-expotential decay ($V_{sf} = V_{sf0} + Ae^{-t/\tau}$) with a time constant $\tau = 0.8$ s, while the transient of the nonpassivated FET contains a fast decay in the beginning followed by a slow tail that does not fit with a single exponential. Instead, it fits well with a sum of two exponentials ($V_{sf} = V_{sf0} + A_1e^{-t/\tau_1} + A_2e^{-t/\tau_2}$). If we fix the time constant of one exponential to be $\tau_1 = 0.8$ s, then the time constant of the other exponential is fitted to be $\tau_2 = 6.2$ s. Compared with the DOS results shown before, we can attribute the 0.8 s decay in both the nonpassivated and passivated FETs to the charge trapping in the bulk oxide, while attributing the 6.2 s slow decay to the surface $-$OH group related trap states on the nonpassivated FET.

The transient surface potential measurements were performed at different spots on the channel region of several different D5TBA crystalline islands on both the nonpassivated and APTES-passivated FETs, with reproducible results, regardless of the distance from the measurement spot to the source/drain electrode. This means that the surface potential transients are due to the local capacitive charge trapping behavior instead of the contact resistance (which varies for different D5TBA islands[20]) or the resistance due to the domain boundaries of the D5TBA and that the charge traps are uniformly distributed in the D5TBA crystalline islands (on the oxide). Furthermore, our previous study shows that the contact resistance of a nonplanar D5TBA FET is on the order of 100 GΩ.[20] If we estimate that the area of a D5TBA island is 1 μm^2, the corresponding oxide capacitance would be around $1 \times 10^{-16}F$, and the *RC* time constant would be on the scale of 10 μs. This again indicates that the contact resistance is not causing the observed surface potential hysteresis, which is on the scale of seconds.

CONCLUSIONS

In conclusion, we have used Kelvin probe force microscopy to measure the surface potential distribution across a D5TBA submonolayer FET. Surface potential−gate bias spectroscopy is performed at local spots on the D5TBA channel of the nonpassivated and APTES-passivated FET, from which the density of band gap electronic states is extracted. Our results show that the nonpassivated FET has a large density of trap states with a Gaussian distribution peaking at 4.2 eV below the vacuum level. This Gaussian peak is eliminated after APTES passivation. Furthermore, we performed transient surface potential measurements showing that the nonpassivated FET has a much larger charge trapping hysteresis than the APTES-passivated FET. These results demonstrate that the gate oxide contains charge trap states located in the bulk and states located at the surface, likely in the $-$OH groups. We further demonstrate that the surface states can be eliminated by suitable passivation with APTES while the bulk states remain unmodified. Our results also

demonstrate that KPFM is a promising tool to characterize local charge trapping behavior of weakly conducting semiconductor thin films with strong charge carrier localization.

METHODS

Fabrication of FET. Heavily doped p++ Si(100) wafer with 300 nm thermal oxide was purchased from Addison Engineering, Inc. The p++ silicon is used as gate. Subsequent source/drain electrode fabrication is done in the nanolab at UC Berkeley. Specifically, UV photolithography is used to pattern the substrate, after which 5 nm Ti and 50 nm Au is deposited, and photoresist lift-off is done using acetone. The fabricated wafer is cleaved into 1 cm × 1 cm pieces, each containing about 50 FETs. Afterward these pieces are sonicated in acetone (10 min) and isopropyl alcohol (10 min) and oxygen plasma cleaned for 1 min. These clean FET substrates are used for either direct Langmuir–Blodgett deposition of D5TBA or APTES deposition and subsequent LB deposition of D5TBA.

APTES Deposition. The cleaned FET substrates are immersed in a solution of APTES in toluene (10 mM) for 2 h within a closed jar in a nitrogen glovebox at room temperature. Subsequently, they are washed by sonication in toluene three times (2 min each). The dried APTES-modified substrates are then stored for 2 h in an oven at 130 °C before being stored under vacuum to remove residual solvent.

Kelvin Probe Force Microscopy. KPFM is implemented using an Agilent 5500 AFM and HF2LI lock-in amplifier (with a built-in PID controller) from Zurich Instruments. We use Cr/Pt-coated AFM tips with 3 N/m force constant and ω_0 = 75 kHz resonance frequency, purchased from BudgetSensors. During the KPFM measurement, a dc bias plus an ac modulation bias with frequency ω = 2 kHz and amplitude of 2 V is applied to the tip. The phase shift signal from the AFM controller is fed to the input of the lock-in amplifier to extract the signal with ω = 2 kHz, which is adjusted to zero by tuning the dc tip bias using a PID feedback loop. The dc tip bias is recorded as the surface potential of the sample. All the AFM images are analyzed using WSxM software.[36] To check that the KPFM measurements on FET are working properly, we perform $V_{sf}-V_g$ spectroscopy on the oxide region of a bare nonpassivated FET substrate (with no D5TBA on top). The result is shown in Figure S4. We can see that the surface potential increases linearly with the gate bias with a slope of 1.0, confirming that the KPFM surface potential measurement is accurate and that the oxide is insulating.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: UV–vis spectrum of D5TBA; XPS N 1s peak of APTES; AFM/KPFM images of APTES; surface potential–gate bias spectroscopy on the oxide of a bare FET substrate. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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