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Electron-Beam Patterning of Polymer Electrolyte Films To Make Multiple Nanoscale Gates for Nanowire Transistors

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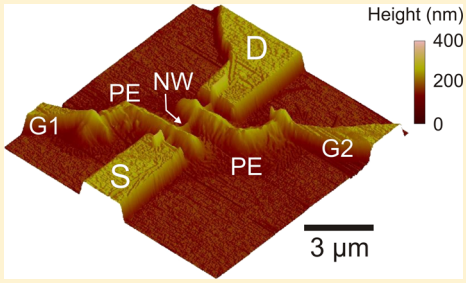
S *Supporting Information*

ABSTRACT: We report an electron-beam based method for the nanoscale patterning of the poly(ethylene oxide)/$LiClO_4$ polymer electrolyte. We use the patterned polymer electrolyte as a high capacitance gate dielectric in single nanowire transistors and obtain subthreshold swings comparable to conventional metal/oxide wrap-gated nanowire transistors. Patterning eliminates gate/contact overlap, which reduces parasitic effects and enables multiple, independently controllable gates. The method's simplicity broadens the scope for using polymer electrolyte gating in studies of nanowires and other nanoscale devices.



KEYWORDS: *III−V nanowires, polymer electrolytes, electron beam lithography, nanoelectronics*

Polymer electrolytes[1] and III−V nanowire transistors[2,3] are two exciting outcomes of recent research on nanoscale devices and novel electronic materials. A polymer electrolyte typically consists of a salt dissolved in a solid polymeric matrix, for example, $LiClO_4$ in poly(ethylene oxide) (PEO);[4] they are commonly used as a gate dielectric in organic field-effect transistors. The electric field resulting from a voltage applied to the gate drives motion of Li^+ and ClO_4^- ions through the polymer matrix to form an electric double layer (EDL) at the gate/insulator and insulator/channel interfaces. EDL formation effectively transfers the gate charge to ~1 nm away from the channel,[5] producing the high dielectric constants and specific capacitances for which polymer electrolyte gate dielectrics are known.[1] The benefits of reduced operating voltages[6] and enhanced carrier density[7] that polymer electrolytes bring to organic transistors have seen them applied to one-dimensional nanomaterials also, first with carbon nanotubes,[8−10] and more recently, with self-assembled InAs nanowires.[11] The latter is part of a broader quest to improve electrostatic gate control in nanowire-based devices, both for fundamental transport studies and potential nanowire device applications.

The first nanowire transistors were gated using a SiO_2-coated, degenerately doped Si substrate; though effective, this approach provides no local control over carrier density.[12] Subsequent work led to patterned local gating of laterally oriented nanowires via electrodes both under[13] and over[14] the nanowire, and more recently, with a concentric "wrap-gate".[15,16] Wrap-gates provide more homogeneous carrier depletion and better gate/channel coupling,[17] give improved subthreshold characteristics and reduced operating voltage,[15,16,18] and enable more controllable devices for fundamental studies of 1D transport.[19−21]

Liang and Gao's use of a PEO/$LiClO_4$ polymer electrolyte gate spin-coated over an InAs nanowire provides a simpler route to lateral wrap-gated nanowire transistors;[11] however, a key limitation resides in a lack of methods for nanoscale patterning of polymer electrolytes. Patterning the polymer electrolyte is desirable to avoid it overlapping the source/drain contacts, which can lead to parasitic capacitance, leakage currents, and contact corrosion.[1] It also enables independent contacting of multiple devices on the same chip. The micrometer-scale resolution of established polymer electrolyte deposition methods, for example, inkjet printing,[22,23] injection into microfluidic channels,[10] and photolithography,[24] presently limits the use of polymer electrolytes in nanowire transistors, where 200 nm to 3 μm channel lengths are typical. Here we report the development of a process for electron-beam patterning of the PEO/$LiClO_4$ polymer electrolyte and demonstrate the versatility it provides by making nanoscale-patterned single and double electrolyte-gated nanowire transistors. This nanoscale patterning capability enables us to produce multiple independent devices, each with multiple independently controllable electrolyte gates, on a single chip.

Electron beam lithography (EBL) is a widely used tool for nanoscale patterning; it relies on using electron-induced chain

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scission/cross-linking to locally alter the solubility of a polymeric resist layer in a developer solution. PEO can be cross-linked by exposure to energetic electrons, which makes these regions comparatively insoluble in developers such as tetrahydrofuran, methanol, and H_2O; as such PEO is a negative-tone EBL resist, though not widely used practically. Krsko et al. first demonstrated EBL of PEO,[25] with feature sizes down to ~200 nm achieved soon thereafter.[26] These works used PEO with molecular weights (MW) of 6.8 and 200 k without any added salts, and 10 keV electrons at doses 1−200 C/m^2. In implementing EBL-patterning of a polymer electrolyte there are some new concerns that arise, for example, whether the added salt either captures incident electrons or adversely affects electron-induced cross-linking, and whether the cross-linked PEO remaining after development has sufficient ionic mobility to produce a functional device. While EBL patterning of salt-doped PEO for nanoscale functional polymer electrolyte gates has not been previously demonstrated, prior research suggests its viability, for example, electron-beam cross-linking has been used to enhance ionic conductivity in solid polymer electrolytes for battery applications.[27,28]

In this work, polymer electrolytes were formed by mixing PEO (Aldrich, MW 100 k) and $LiClO_4{\cdot}3H_2O$ (Aldrich) in polymer−salt ratios of 10:1, 8:1, and 2.4:1 by sonication in 10 mL of methanol. The resulting mixture was left standing at room temperature overnight to precipitate out large particulates, with the supernatant used for deposition. The solution was spun onto the sample at 4000 rpm for 60 s, and the sample was then baked on a hot-plate at 90 °C for 30 min. The resulting film was EBL patterned using either an FEI Sirion for preliminary experiments (Figure 1) or a Raith 150-Two for nanowire device fabrication (Figures 2−4). Patterning was performed using a 5 kV accelerating voltage and beam currents of 20−25 pA under high vacuum. The patterned films were developed in deionized water at room temperature for ~30 s and dried with N_2 gas.

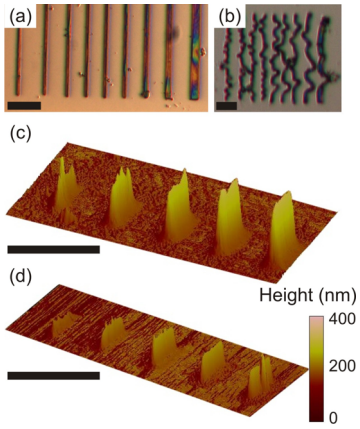

Figure 1. (a,b) Optical micrographs of PEO/$LiClO_4$ patterned by EBL into 50 μm long lines of defined width w_d = 100, 150, 200, 300, 400, 500, 750, 1000, and 2000 nm. The dose in (a) was 4 C/m^2, and the measured line width saturates below defined widths of 500 nm. The dose in (b) was 1 C/m^2: low doses occasionally resulted in pattern distortion during development. (c,d) Atomic force micrograph of 4 μm long lines of defined width 100 nm, with doses of 0.5, 1, 2, 3, and 4 C/m^2 with polymer−salt ratios of (c) 10:1 and (d) 2.4:1. All patterns are on Si substrates. The black scale bars represent 15 μm. Cross-sectional line scans of (c,d) are shown in Figure S1 of the Supporting Information.

The optical micrograph in Figure 1a shows 10:1 PEO/$LiClO_4$ patterned at an electron dose d = 4 C/m^2 into lines with different defined line widths, aimed at establishing the patternability of PEO/$LiClO_4$ films using EBL, and an initial assessment of resolution limit. Pattern broadening is common for negative tone EBL resists and is caused by the proximity effect—the same physics produces the undercut profile for positive tone EBL resists such as polymethylmethacrylate (PMMA).[29,30] This means that the final pattern dimensions can be significantly greater than the region scanned by the electron beam. Thus, two line widths are important: the defined line width, w_d, as written by the electron beam, and the measured line width after development, w_m, which we take as the full width at half-maximum determined by atomic force microscopy. The proximity effect can also result in w_m depending strongly on dose: This is suggested in Figure 1a, where there is a clear difference in measured line width w_m for wider lines (w_d = 750−2000 nm), but w_m saturates for $w_d \leqslant$ 500 nm with d = 4 C/m^2. We used atomic force microscopy to study the effects that the electron dose, polymer−salt ratio, and substrate material have on the shape and dimensions of structures remaining after development.

Figures 1c,d show w_d = 100 nm lines exposed at d = 0.5−4 C/m^2 for two polymer−salt ratios 10:1 (Figure 1c) and 2.4:1 (Figure 1d). Focusing first on dose, in Figure 1c w_m decreases continuously from 1.2 μm to 820 nm as d is reduced from 4 C/m^2 to 0.5 C/m^2. This is expected for proximity effect controlled line-width. Looking more closely at the base-broadening, the width at the substrate can be up to 2 × w_m, but the profiles in Figure 1c show that most of the broadening occurs for heights <50 nm above the substrate surface. This suggests the broadening arises due to surface effects, and as such, the base width may be controllable with surface treatments; we will address this in future work. The reduction of w_m with lower d would imply that minimizing d is most optimum, but there are two additional factors that weigh against this: line height and surface adhesion. First and foremost, the line height h in Figure 1c decreases with d, from h = 350 nm at d = 4 C/m^2 to 150 nm at 0.5 C/m^2. This aspect is particularly crucial to the application in nanowire transistors because for a nanowire of radius R the electrolyte gate needs to have $h > 2R$ after development to cover the nanowire without discontinuity. This height−dose relationship sets a minimum dose for patterning. Additionally, surface adhesion of the patterned PEO encourages further increases in dose. Figure 1b shows an issue that frequently arises for $d \leqslant$ 1 C/m^2. Here the exposed PEO is insufficiently cross-linked to prevent detachment of defined lines from the substrate; the significant line deformation arises from unrestrained swelling of the PEO due to H_2O uptake during development.[25] This problem becomes particularly prevalent for w_d < 100 nm and/or d < 1 C/m^2.

Small changes in polymer−salt ratio, for example, from 10:1 to 8:1, produced little appreciable pattern change, but as Figure 1d shows, w_m and h reduce substantially for a larger increase in salt content to 2.4:1. This suggests that ionic capture of incident electrons at the expense of cross-linking occurs; this can be mitigated to some extent by an increase in dose. Comparing the left-most line in Figure 1c with the right-most line in Figure 1d suggests that a 5× increase in salt content requires a 8× increase in dose. Finally, we find that w_m for a given w_d and d combination reduces by up to 200 nm on

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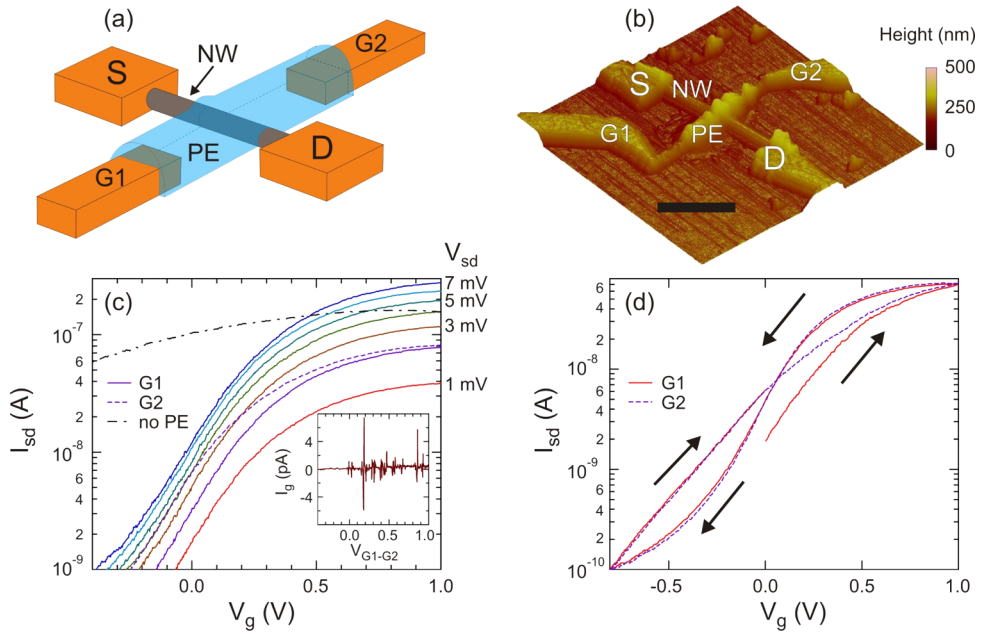

Figure 2. (a) Schematic and (b) atomic force micrograph of a polymer electrolyte-gated nanowire transistor. The components are labeled: source (S), drain (D), nanowire (NW), polymer electrolyte (PE), and gate electrodes (G1 and G2). The black scale bar represents a horizontal distance of 3 μm. (c) Source–drain current I_{sd} vs gate voltage V_g with V_g applied to G1 (solid lines) and G2 (dashed line) of a device with a separation S_{G2} = 2 μm between gate electrode 2 and the nanowire, and G1 for a device with no PEO/$LiClO_4$ (dot–dash line). Traces are shown for V_{sd} = 1–7 mV. Data were obtained with a V_g sweep rate of 5 mV/s from positive to negative. Inset to (c) shows the current I_g flowing between G1 and G2 when a voltage V_{G1-G2} is applied between them. (d) Gate hysteresis at a sweep rate of 5 mV/s for V_g applied to G1 (solid line) and G2 (dashed line) for a device with S_{G2} = 4 μm.

moving from a Si substrate with native oxide only to an n^+-Si substrate capped with 100 nm thermal oxide and 10 nm HfO_2 deposited by atomic layer deposition. The line detachment effect in Figure 1b also becomes less prevalent for the HfO_2/SiO_2-capped substrates used in nanowire processing. These improvements may be due to improved adhesion of PEO to the substrate surface and modification of the electron beam interaction volume due to the layered oxide structure,[31] combined with the much higher electrical conductivity of the underlying Si. There may be scope for further improvement in resolution, e.g., with added reagents for controlling cross-linking. A line width of 500–1000 nm is sufficient to gate the 3–6 μm long InAs nanowires we use here without electrolyte/contact overlap, so we leave this further process development for future work and now turn to the nanowire devices.

Figures 2a,b show a nanowire transistor incorporating a single polymer electrolyte gate (PE) connected to two Ni/Au gate electrodes (G1 and G2). The second electrode was used to test whether the electrode–nanowire separation, S_{G1} or S_{G2}, influences PE gate operation; electrodes G1 and G2 are separated from the nanowire by S_{G1} = 1 μm (fixed) and S_{G2} = 1–4 μm (varied between devices), respectively. The PE gate has a polymer–salt ratio of 10:1 and was written with w_d = 100 nm and d = 1 C/m^2, giving a strip with w_m = 650 nm and $h \sim$ 130 nm. Figure 2c shows the source–drain current I_{sd} versus PE gate voltage V_g for seven different source–drain biases V_{sd} between 1 and 7 mV with V_g applied to G1 (solid lines) and at V_{sd} = 2 mV with V_g applied to G2 (dashed line). In all experiments, the electrode that did not have V_g applied was kept at ground—however there was no major difference to the transfer characteristics if this electrode was floated (see Supplementary Figure S2a). There is hysteresis in the gate characteristics, as we show in Figure 2d, and discuss further below. Hence for the data in Figure 2c we only show data obtained for one sweep direction: from positive V_g toward more negative V_g. Considering data for V_g applied to G1 first, we obtain a subthreshold swing of 271 mV/decade for data in Figure 2c. Across 12 devices studied so far with a 10:1 polymer–salt ratio (a total of 22 working gates) we obtain an average subthreshold swing 307 ± 33 mV/decade. The average threshold voltage was +0.16 ± 0.06 V at V_{sd} = 2 mV across the 12 devices. We now look at the influence of the separation between the gate electrode and the nanowire on the transistor characteristics. For the device measured in Figure 2d, S_{G1} = 1 μm and S_{G2} = 2 μm. Despite this difference, the gate characteristics in Figure 2c are very similar with almost identical subthreshold swing. We find this same behavior across many devices where S_{G2} ranges from 1 to 4 μm (see Supplementary Figure S2b). The lack of dependence of the subthreshold swing on gate electrode to nanowire separation is not surprising; for an ideal EDL, V_g drops across the nanowire/electrolyte and electrode/electrolyte interfaces, not across the electrolyte itself. The result is that the steady state gate capacitance—and thereby the subthreshold swing—is independent of the electrode-nanowire separation. Note that the polymer electrolyte is not electronically conductive; Figure 2c (inset) shows a plot of current through the PE gate I_g versus potential difference between electrodes G1 and G2 V_{G1-G2} demonstrating a negligible electronic conductivity despite a significant ionic conductivity.

Gate hysteresis is a common issue for transistors incorporating polymer electrolyte gate dielectrics. It normally arises due to the finite ionic mobility of the polymer electrolyte, since ions need to drift through the polymer to re-establish electrostatic equilibrium at the EDLs when the voltage on the gate electrode is altered. This hysteresis will depend on

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properties of the polymer electrolyte, but also on the distance between the gate electrode and transistor channel. On its own, the delay imposed by ion migration means that I_{sd} for sweeps from positive (negative) to negative (positive) gate voltages will be higher (lower) than otherwise expected, producing a counter-clockwise hysteresis loop. Figure 2d shows extended I_{sd} vs V_g traces for G1 (solid red line) and G2 (dashed purple line) for a device with S_{G1} = 1 μm and S_{G2} = 4 μm. Two interesting features are evident. First, neither gate trace follows a simple, counter-clockwise cyclical loop; instead they take a "figure of 8" form that indicates possible additional contributions to the hysteresis. One additional contribution may be charge trapping by nanowire surface states,[18,32] which would depend on the exact nature of the InAs/PEO interface. Second, aside from the "virgin" behavior in the initial positive ramp of G1, the hysteresis traces for G1 and G2 are identical, despite the factor of 4 difference between S_{G1} and S_{G2}. While the gate response is not identical for all devices, there is no clear relation between the magnitude of the hysteresis and S_{G2}. This also points to contributions other than ionic mobility to the hysteresis and suggests that these other contributions are dominant. Indeed, much smaller hysteresis loops are typically seen in organic transistor and carbon nanotube devices with PEO/$LiClO_4$ gate dielectrics.[10,33] We characterize the hysteresis further in the Supporting Information, but most notably, the hysteresis can be reduced significantly by sweeping over a smaller gate range and/or at a lower rate. Determining the relative contributions of ionic mobility, surface states and other possible contributions to the gate hysteresis is beyond the scope of this work but would be an interesting subject for future studies.

We now consider the effect of increased salt content on the device structure in Figure 2a,b. The first place where this presents an effect is in device fabrication. Unlike the test structures in Figure 1, here we need to precisely align the PE gate to the gate electrodes and nanowire, and this is done by briefly viewing metal alignment markers on the substrate immediately prior to EBL patterning to ensure correct pattern alignment. Increasing the polymer−salt ratio to 8:1 makes the PEO/$LiClO_4$ film opaque to the electron beam, resulting in difficulties in pattern alignment and thereby dramatically reducing device yield. Interestingly, increasing the polymer−salt ratio to 2.4:1 returns some of the PEO/$LiClO_4$ film's transparency to an electron beam—we explain this below. The second place where we see a salt concentration effect is in the electrical characteristics. Despite reduced yield, we successfully measured four devices at 8:1 obtaining an average subthreshold swing of 286 ± 45 mV/decade from eight gates. We also measured four devices at 2.4:1 obtaining an average subthreshold swing of 431 ± 53 mV/decade from eight gates measured. Both the maximal electron beam opacity of the PEO/$LiCLO_4$ film and the maximal subthreshold swing at an intermediate polymer−salt ratio can be explained by the "ionic conductivity peak" observed as a function of salt concentration;[34] this peak typically occurs at 8:1.[35] Thus we have concluded that a 10:1 polymer−salt ratio offers the best compromise between patternability and device performance for the remainder of this work.

Comparing the performance of our PE gated devices to other nanowire transistors, our typical subthreshold swing of ∼300 mV/decade compares very favorably with substrate-gated nanowire transistors, where subthreshold swings of order 1−4 V/decade are typical.[15] The performance is also competitive with metal/oxide wrap-gated nanowire transistors, where subthreshold swings typically range from 100 to 750 mV/decade.[15,18,36−39] This is particularly impressive as the polymer electrolyte does not completely wrap around the nanowire in our devices, unlike in ref 11 where a HF etch was used to undercut the nanowire to provide access for the PEO/$LiClO_4$ film. This undercut etch was impractical to implement here as our HfO_2 cap layer is much more resistant to HF etching than SiO_2;[15] this step could easily be implemented for substrates with a thermally grown SiO_2 layer alone.

A concern that could be raised is that closely positioned, biased metal electrodes can also influence nanowire conduction.[40] Since we observed evidence for some electron capture by Li^+ ions at the patterning stage, the question that naturally follows is: To what extent does the direct coupling of the metal electrodes to the nanowire contribute to modulation of I_{sd} with V_g? For example, is it that Li^+ ions are neutralized by incident electrons during EBL such that ionic conduction is a cocontributor with electrostatic repulsion via the gate electrodes, rather than the dominant contributor to channel depletion? The black dot−dash trace in Figure 2c shows the characteristics for a device like that in Figure 2a,b, but without any PEO/$LiClO_4$. At V_g = −0.4 V the bare electrode has only reduced I_{sd} by a factor of 2 compared to factor of $>10^2$ for the PE-gated device. Pinch-off can be achieved with a bare electrode, but it requires $V_g \sim -3$ V with S_{G2} = 1 μm and a much more negative V_g at greater electrode−nanowire separations. This is expected, since there is no EDL formation for bare electrode gating. The behavior of the bare electrode suggests that EDL formation is the dominant contributor to channel depletion in devices with a polymer electrolyte, despite any ionic mobility loss or neutralization that may arise from the EBL process. We confirm this via one final test with our dual PE-gated devices, which we now discuss.

Figures 3a,b show a PE-gated device with two independent gates. Here, we have located the electrodes G1 and G2 such that their direct electrostatic coupling to the nanowire is screened by the source/drain contacts. This ensures that all depletion in this device arises from EDL formation by ion migration in the polymer electrolyte, which had a polymer−salt ratio 10:1. Figure 3c shows I_{sd} versus V_g for G1 (solid lines) and G2 (dashed lines) for several different V_{sd}. The characteristics for the two gates are similar, with G1 and G2 giving subthreshold swings of 332 and 321 mV/decade, respectively. These values are within error for the average values obtained from the single gate devices. This demonstrates that direct coupling to the metal electrodes makes a negligible contribution to depletion and that consistent performance can be obtained from our PE gate structures. The dotted line in Figure 3c shows the characteristics obtained when V_g is applied to both G1 and G2 simultaneously. The subthreshold swing improves to 192 mV/decade, suggesting that performance gains might be achieved in our single PE-gate transistors by careful adjustment of gate width.

To better assess the control, balance, and temporal stability of these gates, and gauge the potential for making more complex devices, for example, a single electron transistor, we performed a more in-depth study of the two gates in our dual PE-gate transistor device when used within an operating range with relatively low hysteresis. This involved taking the device in Figure 3b through a "program" where G1 and G2 were swept together or separately between two predefined voltages V_A = −200 mV and V_B = 0 V. The program for G1 and G2 versus

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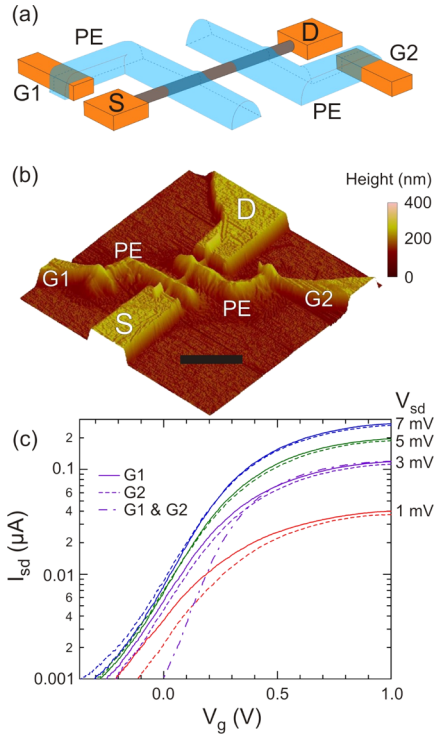

Figure 3. (a) Schematic and (b) atomic force micrograph of a dual PE-gated nanowire transistor. The source (S), drain (D), polymer electrolytes (PE), and gate electrodes (G1 and G2) are labeled. The black scale bar represents a horizontal distance of 3 μm. (b) Source–drain current I_{sd} vs gate voltage V_g for the device in (a) for G1 (solid lines), G2 (dashed lines), and G1 and G2 biased together (dot–dash line). Traces are shown for V_{sd} = 1, 3, 5, 7 mV and obtained with a V_g sweep rate of 5 mV/s from positive to negative voltage.

time t is shown in Figure 4a and b, respectively, with the I_{sd} response plotted in Figure 4c. The full program takes 50 min, and the program is paused after each gate sweep to check stability for 30 s (black segments). The program produces an I_{sd} that alternates between three distinct current states I_{high}, I_{mid}, and I_{low}, which correspond to three gate configurations: $V_{G1} = V_{G2} = V_B$; $V_{G1} = V_A$, $V_{G2} = V_B$ or $V_{G1} = V_B$, $V_{G2} = V_A$, and $V_{G1} = V_{G2} = V_A$. The fact that $I_{sd} = I_{mid}$ for both $V_{G1} = V_A$, $V_{G2} = V_B$ and $V_{G1} = V_B$, $V_{G2} = V_A$ highlights the strong electrical balance between the two nominally identical patterned PE gates. Further, the consistent return to I_{high}, I_{mid}, and I_{low} across the program in Figure 4 demonstrates the stability and low gate drift of this device within this operating region.

One could equally view Figure 4 as a demonstration of two-gate logic, where we set input states [1, 1] ($V_{G1} = V_{G2} = V_B$), [1, 0] ($V_{G1} = V_B$, $V_{G2} = V_A$), [0, 1] ($V_{G1} = V_A$, $V_{G2} = V_B$), and [0, 0] ($V_{G1} = V_{G2} = V_A$) giving either AND or OR operations as output if the threshold is set above or below I_{mid}, respectively. While logic is in principle possible in this device, the time response of the polymer electrolyte gates is insufficient to be competitive for applications. The data in Figure 4 represent the fastest operation we can presently achieve, that is, a few mV/s, without compromising on stability and reproducibility in I_{sd} of the logic states. For faster sweeps, the current at each state is less stable over the 30 s period, and the value of the current at each state varies throughout the program. This makes each state less distinct and limits the practical switching speed to less than 1 Hz. There is some scope for improving the switching speed in future work by passivation of surface states, or engineering of the polymer electrolyte, for example, by optimizing PEO/$LiClO_4$ salt content or adding plasticisers/nanoparticles.[41−43] While switching speeds from 1 to 100 Hz have been obtained in devices incorporating solid polymer electrolytes such as PEO/$LiClO_4$, speeds up to 10 kHz can be obtained by moving to a special class of polymer electrolytes known as "ion gels".[1,23,44−45] These consist of an ionic liquid, that is, a room-temperature molten salt, dispersed in a gel matrix typically formed using a block copolymer. A common example is 1-ethyl-3-methylimidazolium bis-(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) in poly-(styrene-*block*-ethylene oxide-*block*-styrene).[23] A first step may be to attempt EBL patterning of PEO-containing ion gels;[24,44,45] however, it is possible these would suffer the same resolution difficulties described above. Another candidate may be PMMA-based ion gels:[23,46] PMMA is a high resolution negative-tone resist under very high electron doses, with feature sizes as small as 150 nm reported.[47] This could potentially solve both the resolution and switching speed problems encountered

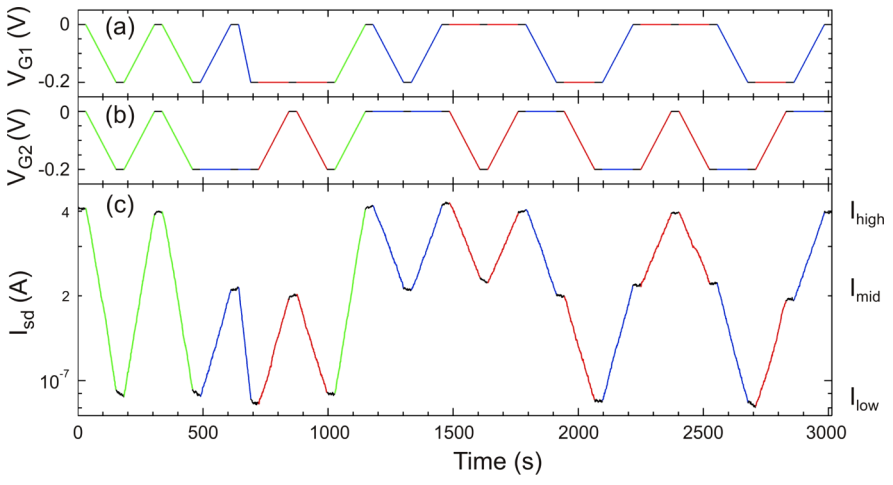

Figure 4. (a) V_g on G1, (b) V_g on G2, and (c) I_{sd} vs time t with constant V_{sd} = 42 mV demonstrating independent operation of the gates on the dual polymer electrolyte-gated nanowire device. To highlight the actions, trace segments are colored: green = G1 and G2 swept together, blue = G1 swept with G2 fixed, red = G2 swept with G1 fixed. The stability of the resulting I_{sd} was monitored for 30 s at the end of each sweep in the program (black sections). Gates were swept at 2 mV/s.

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here and lead to nanoscale electrolyte gates with high resolution, ionic conductivity, and switching speed. Nevertheless, the patterned PEO/$LiClO_4$ polymer electrolyte is an effective gate dielectric for applications where a strong field is required but fast switching speeds are not.

In conclusion, we have demonstrated electron-beam patterning of PEO/$LiClO_4$ electrolyte that allows gating of individual InAs nanowires with single or multiple independently controllable gates without gate/contact overlap. The electrolyte facilitates strong gate-channel coupling; the subthreshold swing of our devices is comparable to that of wrap-gated devices and tends to improve with greater channel coverage. The fabrication of these devices is simpler than for wrap-gated devices: only one extra EBL step is required compared to traditional substrate-gated nanowire transistors. Our dual PE-gated devices exhibit independent gate control and ability to perform basic logic operations.

Materials and Methods. *Fabrication.* Nanowire devices were fabricated from 3 to 6 μm long, 50 nm diameter InAs nanowires grown by MOCVD. Devices were fabricated on 0.001−0.005 Ω·cm As-doped (100) Si wafer (Silicon Valley Microelectronics) with a 100 nm thermal oxide and an additional 10 nm HfO_2 layer deposited by atomic layer deposition. This wafer was prepatterned with Ti/Au interconnects and EBL alignment structures before being divided into smaller "chips" on which nanowire transistors were made. Nanowires were deposited by dry transfer using a lab wipe. Source, drain, and gate electrodes were then defined by EBL using a Raith 150-two system. The EBL resist was a 5% solution of 950k MW PMMA in anisole (Microchem) deposited by spin coating at 5000 rpm followed by a 5 min hot plate bake at 180 °C, developed using a 1:3 mixture of methylisobutylketone in 2-propanol. The electrodes consisted of 25 nm Ni and 75 nm Au deposited by thermal evaporation, immediately after a 120 s $(NH_4)_2S_x$ contact passivation step at 40 °C.[48] Lift-off was performed overnight in *N*-methyl-2-pyrrolidone at 80 °C. Following lift-off, a PEO/$LiClO_4$ film was spin-coated, baked, and patterned by EBL as described in the main text to produce completed devices, which were then packaged in LCC20 ceramic chip carriers (Spectrum) and bonded using an Au ball bonder (Kulicke & Soffa 4500). Atomic force microscopy (AFM) studies were performed prior to packaging using a Dimension DI-3000 AFM in tapping mode using Veeco OTESPA7 probes. AFM was performed in a cleanroom ambient atmosphere (temperature 20 °C and relative humidity 50−60%).

Electrical Characterization. All electrical characterization presented here was performed at room temperature and atmosphere. The source−drain current was measured using a Stanford Research Systems SRS830 lock-in amplifier with an a.c. excitation V_{sd} = 1−50 mV applied at a frequency of 73 Hz using the internal oscillator. Gate electrodes were biased to V_g using Yokogawa GS200 or Keithley 2400 voltage sources with built-in current monitoring for tracking the gate leakage current. The gate current I_g in the inset of Figure 2c was monitored by a Keithley 6517A electrometer.

Devices were stored in the dark in vacuum between measurements to preserve the quality of the ohmic contacts[48] and polymer electrolytes. Under these conditions, device characteristics typically remained reproducible for a period of 3−4 months before beginning to degrade (see Supplementary Figure S4).

■ ASSOCIATED CONTENT

Supporting Information

Additional supporting data on line-width studies as well as device characteristics, hysteresis, and longevity. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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