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Conjugated-Polymer-Based Lateral Heterostructures Defined by High-Resolution Photolithography

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Solution processing of polymer semiconductors provides a new paradigm for large-area electronics manufacturing on flexible substrates, but it also severely restricts the realization of interesting advanced device architectures, such as lateral heterostructures with defined interfaces, which are easily accessible with inorganic materials using photolithography. This is because polymer semiconductors degrade, swell, or dissolve during conventional photoresist processing. Here a versatile, high-resolution photolithographic method is demonstrated for patterning of polymer semiconductors and exemplify this with high-performance p-type and n-type field-effect transistors (FETs) in both bottom- and top-gate architectures, as well as ambipolar light-emitting field-effect transistors (LEFETs), in which the recombination zone can be pinned at a photolithographically defined lateral heterojunction between two semiconducting polymers. The technique therefore enables the realization of a broad range of novel device architectures while retaining optimum materials performance.

1. Introduction

Direct-write printing and solution processing of polymer semiconductors is being pursued as a new paradigm for large-area electronics manufacturing on flexible substrates.[1–3] However, for many applications the reliability and resolution achievable with printing is as yet insufficient and commercialization is held back by the incompatibility of conjugated polymer materials with established manufacturing techniques such as photolithography. Soluble polymers swell, dissolve, and degrade when exposed to common resist and aqueous developer chemicals.[4–6] Photolithographic patterning is particularly challenging for device configurations which rely on the electronic properties of the top surface of the organic semiconductor. If one attempts, for example, to pattern the active semiconductor layer of a top-gate organic field-effect transistor (FET) by standard photolithography prior to deposition of the gate dielectric, severe device degradation is observed, because there are no suitable techniques to clean the surface of the organic semiconductor after it becomes contaminated by photoresist or developer residues. Patterning of the active semiconducting layer is essential to reduce cross-talk, leakage currents, and parasitic channels between devices in integrated circuits. Similarly, techniques are needed that allow realization of well-defined lateral heterojunctions between two polymers without the solution deposition and patterning of one of the polymers degrading the optoelectronic properties of the other polymer. An example would be an ambipolar light-emitting field-effect transistor (LEFET), in which one could optimize performance by defining in the plane of the substrate separately layers for hole and electron transport as well as light emission.[7–9] For inorganic and insoluble, vacuum-sublimed organic semiconductors, such junctions are the basis of many advanced optoelectronic device architectures.[10–12] Here we introduce a simple, versatile, high resolution, and clean photolithographic patterning method, which can be applied to all common TFT architectures as well as a wide range of solution-processed organic semiconductors without device degradation and allows precise alignment of the semiconductor pattern with respect to previously defined electrodes and other substrate structures. Recently, a similar patterning method was developed independently.[13]

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2. Results and Discussion

2.1. Patterning Method

Our patterning process comprises three main steps (**Figure 1a**): i) deposition of a sacrificial polymer layer on top of the surface of the organic semiconductor layer to be patterned (step 1); ii) conventional photolithography followed by wet or dry etching of the organic semiconductor to define the high-resolution pattern (steps 2–6); and iii) removal of the sacrificial layer (step 7). The requirements for the sacrificial polymer layer are stringent. Its deposition should not degrade the surface properties of the organic semiconductor, but it should protect the semiconducting layer underneath during the photolithography and etching step. In the areas where the organic semiconductor is

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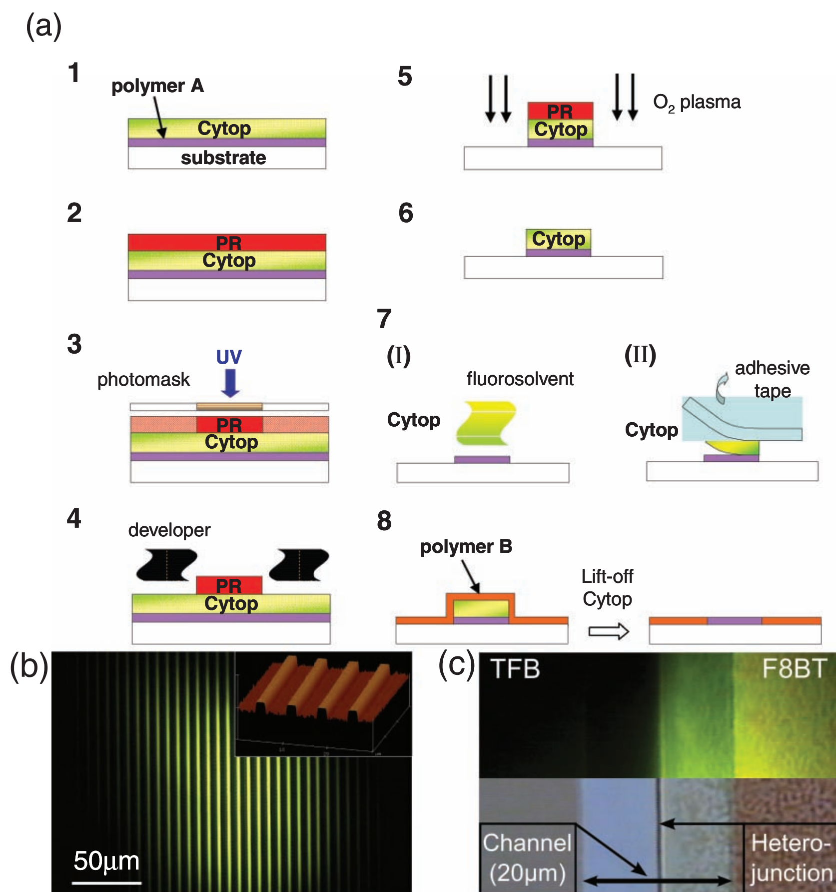

Figure 1. Photolithographic patterning of semiconducting polymer thin films. a) Schematic process flow. A Cytop layer is used as a protective layer (1) of the polymer during photoresist (PR) deposition (2), ultraviolet (UV) exposure (3), development (4), O_2 plasma etching (5), and PR removal with acetone (6). For single-polymer patterning, the Cytop layer can be removed afterward by dissolving in fluorosolvent (7(I)), or by solvent-free, physical delamination with adhesive tape (7(II)). For patterning of lateral polymer heterostructures the patterned Cytop layer can protect the first patterned polymer while depositing the second polymer. Lift-off patterning renders the desired heterostructure (8). b) Photoluminescence (PL) image of patterned F8BT stripes with 2 µm ridge width and 5 µm spacing. The Cytop on top of the F8BT ridges is removed by dissolving in fluorosolvent. The inset shows a tapping-mode atomic force microscopy (AFM) surface topography image. c) PL and optical microscope image of an F8BT/TFB heterojunction within the FET channel.

to be removed it needs to be etched by the same etch method as used for the organic semiconductor. Here we use oxygen plasma etching. Most critically, after patterning it needs to be removed without leaving any residues on the surface of the organic semiconductor. We show here that the perfluorinated polymer Cytop (Asahi Glass Co.) meets all these requirements. Cytop has been used as a low-*k* dielectric in organic FETs[14,15] and for device encapsulation due to its high thermal, chemical, and water resistance.[16] Cytop is an excellent protective layer for the underlying semiconducting polymer against short-time water and developer immersion during the photolithography process. Moreover, Cytop is deposited from fluorosolvents which are highly orthogonal to the solvents for most organic semiconductors. It forms only a very weak interface with negligible degree of intermixing with the organic semiconductor such that it can be removed without residues and without perturbing the surface molecular ordering critical for achieving good device performance. These properties make Cytop superior to previously reported protective layers such as parylene[17] or polyvinyl alcohol (PVA)/poly(methyl methacrylate) (PMMA).[18] For Cytop removal (step 7) we use one of two methods: I) dissolution by a fluorosolvent, or II) peel off with an adhesive tape.

With Method I precisely patterned 1–2 µm wide ridges of polymers such as poly(9,9-di-*n*-octylfluorene-*alt*-benzothiadiazole) (F8BT) (Figure 1b) have been obtained on both hydrophilic and hydrophobic substrates with excellent homogeneity over hundreds of micrometers. The O_2 plasma etching renders very sharp edges and the surface of the patterned F8BT ridges is uniform with a small roughness of ~0.5 nm (see inset) similar to that of pristine F8BT films.[19] The luminescent properties, even near the edge of the pattern, are undegraded. Method II is advantageous for achieving molecularly clean top surfaces of polymer films and can be easily processed in nitrogen atmosphere, which is favorable for materials that are sensitive to the air. It allows patterns with larger features on a 100 µm scale (Figure S1) and is limited to substrates that provide sufficiently strong adhesion with the organic semiconductor.

In the following section, we demonstrate the versatility of this process by applying it to pattern the active semiconductor layer of a broad range of top gate, p-type, n-type, as well as ambipolar organic FETs based on both polymers. This includes several semiconducting polymers that are very prone to processing-induced materials degradation, such as poly-3-hexylthiophene (P3HT) and poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b) thiophene) (PBTTT),[20] which are also easily p-type doped during processing,[21,22] and F8BT,[19] which is capable of ambipolar conduction and realization of ambipolar LEFETs, but for which n-type, electron transport degrades rapidly upon exposure to water/moisture and to the atmosphere.

A particularly powerful attribute of our technique is that it allows fabrication of well-defined lateral heterojunctions between two semiconducting polymers. The patterned structure comprised of polymer A with a Cytop layer after step (6) can be further extended to yield a lateral polymer/polymer heterojunction (step 8). Using solution-processed semiconducting polymers, it has been very challenging to produce a well-defined lateral heterostructure due to the difficulties of controlling interfacial mixture between two polymers by means of solvent deposition. Here, however, the Cytop layer protects the patterned polymer A from solvent attack while depositing polymer B. A well-defined heterojunction is formed after a subsequent delamination/lift-off process of the Cytop layer and the overlying

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undesired polymer B parts. An edge bead can result during the lift-off process, which can, however, be minimized by reducing the Cytop thickness. We illustrate this in Section 2.3 with an ambipolar LEFET (as the image shown in Figure 1c), in which the recombination zone is pinned within the channel at the lateral heterojunction between two semiconducting polymers.

2.2. Electrical Characteristics of Patterned FETs

Our patterning technique can be applied to all common FET architectures. Patterning of bottom-gate devices is comparatively straightforward, because the bulk of the organic semiconductor protects the critical, buried interface during processing. As shown in Figure S2, the characteristics of the patterned PBTTT bottom-gate devices are practically identical to those of unpatterned devices (mobility ~0.1 cm^2 V^{-1} s^{-1}), except for a slightly positive turn-on voltage shift. In fact, lithography using a protective layer, such as a vacuum-deposited film of crosslinked, insoluble parylene, has been used previously to pattern the organic semiconductor layer for such bottom-gate devices.[23,24] Much more challenging, however, is the patterning of top-gate devices, because this requires the ability to cleanly remove the protective layer and to form high-mobility electron and hole accumulation layers on the top surface of the polymer films after patterning. We demonstrate this here for a wide range of semiconducting polymers. Patterned PBTTT (**Figure 2a**) and P3HT (Figure S3b) top-gate transistors have similar on-current but considerably enhanced on/off ratios by 2–3 orders of magnitude compared to the unpatterned devices. The off-current of the patterned devices is reduced to the gate leakage level (10^{-11}–10^{-12} A). The linear mobilities of the patterned/unpatterned PBTTT and P3HT top-gate devices with PMMA gate dielectric are ~10^{-1} and ~10^{-2} cm^2 V^{-1} s^{-1}, respectively. Patterning of top-gate transistors with polyfluorene polymers such as F8BT (Figure 2b and S3c), poly-9,9′-dioctyl-fluorene-*co*-bithiophene (F8T2) and poly(9,9-di-*n*-octylfluorene-*alt*-(1,4-phenylene-((4-sec-butyl-phenyl)imino)-1,4-phenylene)) (TFB, Figure S3d), also results in no evident degradation of the active materials. For F8BT devices with gold electrodes we observe clean ambipolar device characteristics. The patterned device has similar p-type (~6.2 × 10^{-4} cm^2 V^{-1} s^{-1}) and slightly lower n-type (~8 × 10^{-4} cm^2 V^{-1} s^{-1}) saturation mobilities than the unpatterned device. We note that the electron current in F8BT diminishes when using Cytop as the gate dielectric (probably due to prevalent electron traps in the dielectric), while the current recovers to the level of standard PMMA devices after removing Cytop and depositing a PMMA dielectric (Figure 2b). We have also obtained high-performance n-type, top-gate FETs with a naphthalene-bis(dicarboximide) (NDI)-based high-mobility polymer P(NDI2OD-T2) (Figure 2c). The patterned devices show high electron mobilities of 0.1–0.2 cm^2 V^{-1} s^{-1} when using redeposited Cytop as gate dielectric, close to those of unpatterned devices.[25]

We have also compared the reliability and lifetime under bias stress conditions for patterned and unpatterned devices (Figure S4). During a continuous gate bias stress at V_g = −50 V the turn-on voltage of both devices is seen to continuously shift to more negative values. Such threshold voltage shifts are commonly observed in organic FETs and are a manifestation

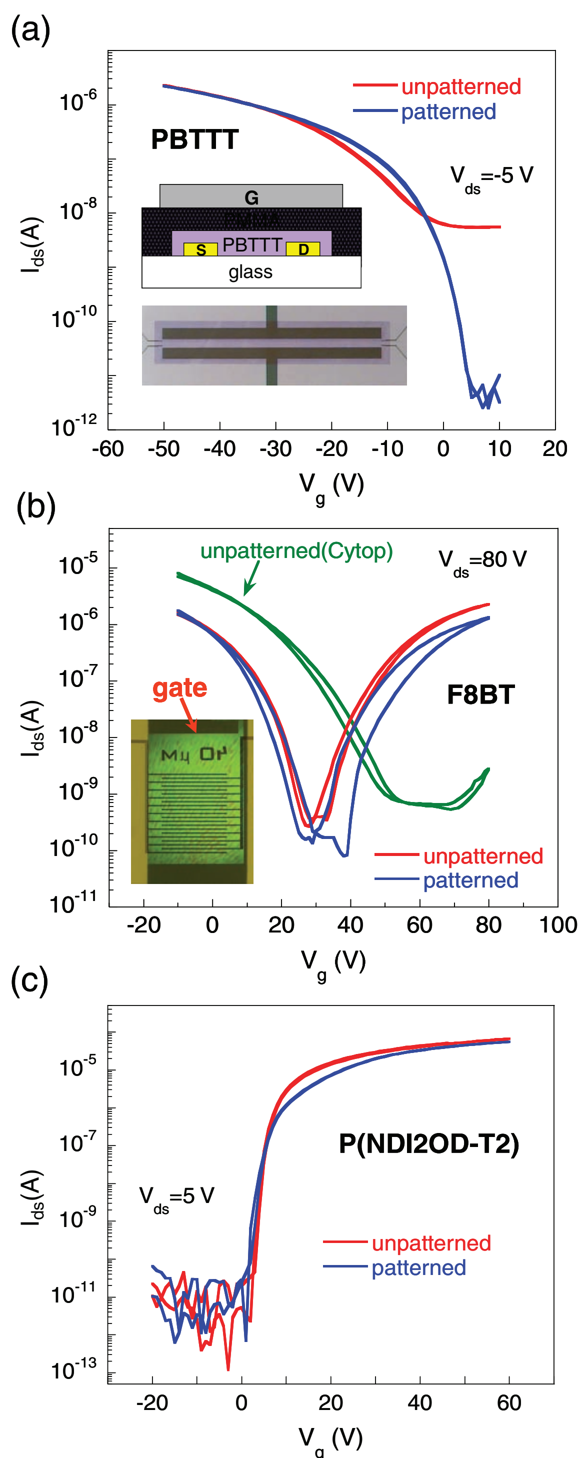

Figure 2. Comparison of patterned and unpatterned FET performance for various polymers. Transfer characteristics of a) p-type PBTTT top-gate/bottom-contact devices (L = 40 µm and W = 1000 µm). The image of the patterned PBTTT and schematic diagram of the device are shown in the inset. b) Ambipolar F8BT top-gate/bottom-contact devices (L = 40 µm and W = 20 000 µm). A 500 nm thick PMMA was used as the gate dielectric for PBTTT and F8BT devices. The device characteristics for an F8BT device with Cytop gate dielectric is also shown. c) n-Type P(NDI2OD-T2) top-gate/bottom-contact devices (L = 40 µm and W = 20 000 µm) with 500 nm Cytop as the gate dielectric.

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of some of the accumulated mobile hole carriers becoming trapped in localized states at the interface.[26,27] However, the degradation of patterned and unpatterned devices was found to be very similar, further demonstrating that the photolithographic processing does not introduce any additional defects or impurities at the interface which could cause accelerated charge trapping and degrade the lifetime of the transistor.

Furthermore, we have applied the process to pattern the two active layers of a complementary inverter based on p-type PBTTT and n-type P(NDI2OD-T2) top-gate FETs (**Figure 3a**, process sequence shown in Figure S5). These two materials can be processed on the same substrate with matched mobilities of ~0.1 cm^2 V^{-1} s^{-1} using PMMA as a common gate dielectric and gold source–drain electrodes. The inverter's static voltage transfer characteristics (Figure 3b) exhibits a nearly complete output voltage swing with good symmetry, high-voltage gains (dV_{out}/dV_{in}) of >10 and noise margins larger than 0.25 × V_{DD}, and makes a robust building block for the integration of logic circuits.

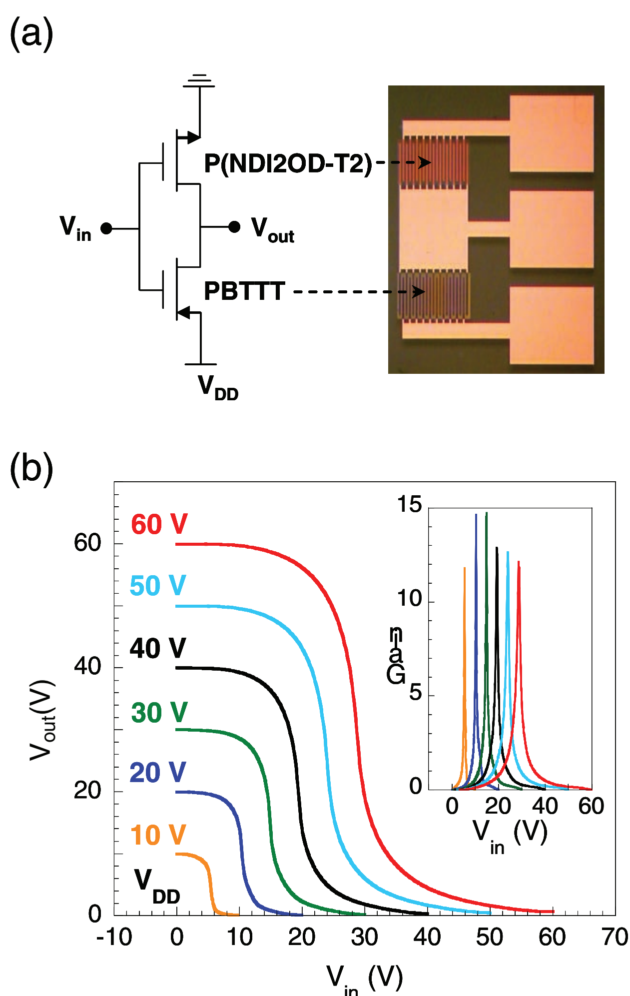

Figure 3. Complementary inverters with patterned p-type PBTTT and n-type P(NDI2OD-T2) FETs. a) Schematic illustration and optical microscope of a complementary inverter with a patterned PBTTT p-type FET and a P(NDI2OD-T2) n-type FET (L = 20 µm and W = 10 000 µm). b) Switching characteristics of the inverter. The inset shows the gain of the inverter as calculated from the switching characteristics.

2.3. Heterojunction LEFETs

As mentioned before, our photolithographic patterning technique also allows fabrication of high-quality lateral heterojunctions with two solution processed, patterned polymer semiconductors in intimate physical contact along a common edge of their patterns. We demonstrate this capability here with a polymer LEFET comprising a well-defined lateral heterojunction between F8BT and TFB positioned within the channel (Figure 1c). This materials system has been commonly used as a blend system or vertical heterojunction for highly efficient LEDs.[28–30] The offsets of the electron affinities and ionization potentials at the heterojunction confine the incoming holes and electrons on the TFB and F8BT side of the heterojunction, respectively. In previous realizations of ambipolar polymer LEFETs with single component semiconductors the position of the recombination zone in the channel could be controlled with the applied voltage,[8] but due to device instability it was difficult to stabilize the recombination zone at a fixed position. Our objective with the LEFETs made here is to demonstrate that the recombination zone can be pinned at the lateral heterojunction and to develop an architecture that allows real-space observation of the carrier confinement at the heterojunction.

To fabricate the junctions we first patterned the F8BT film by photolithography as described above to cover about half of the FET channel (Figure S6). We then deposited the TFB film from a xylene solution with the Cytop sacrificial layer being still on top of the F8BT. Since F8BT is soluble in xylene, the patterned Cytop layer protects the F8BT film from being dissolved in xylene. The lateral heterojunction was then formed by lifting off the TFB film on top of the patterned F8BT together with the Cytop layer. Detailed analysis of the interfacial morphology (reported in the Supporting Information, see Figure S7) shows that the heterojunction is well defined and reasonably abrupt. On the TFB side of the junction a 100–140 nm thick edge bead is produced when the TFB film is lifted off together with the relatively thick layer of Cytop (~1 µm). On the F8BT side of the heterojunction we observe a 2–4 µm wide region, in which the luminescent properties and film thickness of the F8BT are slightly modified due to diffusion of the xylene TFB solvent into the F8BT film (Figure S7). This is consistent with compositional Raman analysis. **Figure 4a** shows a 2D Raman map of the F8BT/TFB heterojunction obtained by confocal Raman microscopy with a 1 µm spot size. The absolute Raman intensity integrated between 1510 and 1570 cm^{-1} was plotted as a function of position near the heterojunction (Figure 4b). The Raman peak at 1544 cm^{-1} corresponds to F8BT and is not present in TFB. On the F8BT side of the heterojunction a typical, pure F8BT spectrum with a characteristic ratio of the fluorene ring stretch peak (1606 cm^{-1}) to the benzothiadiazole ring stretch peak (1544 cm^{-1}) is observed. On the TFB side of the heterojunction a characteristic TFB spectrum is measured comprising peaks due to the (partially resolved) fluorene ring stretch (1606 cm^{-1}) and the phenylene ring stretch (1600 cm^{-1}). These spectra are in excellent agreement with literature.[31–33]

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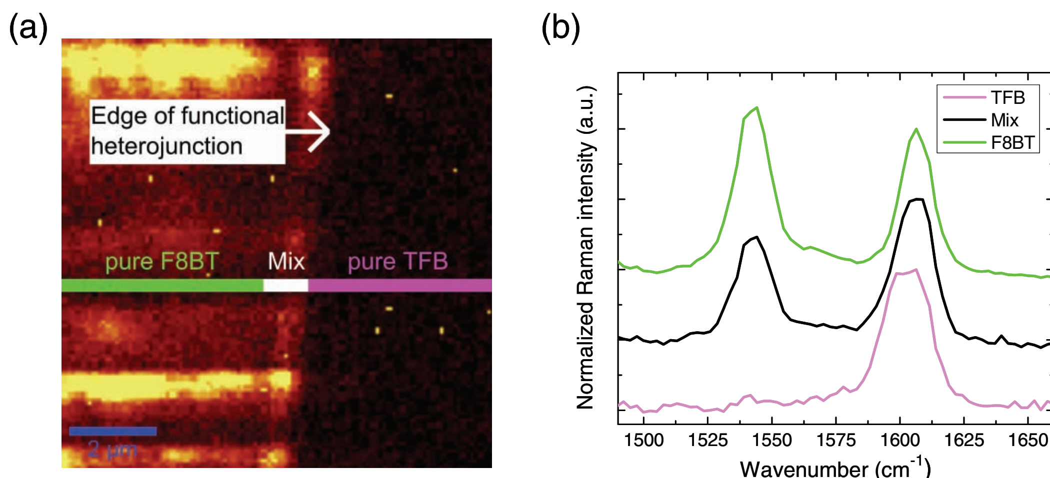

Figure 4. a) 2D Raman map showing the intensity of the benzothiadiazole ring stretch as a function of position in the vicinity of the heterojunction. b) Raman spectra taken on the F8BT and TFB side a few micrometers from the heterojunction and right on top of the heterojunction (mix).

Raman spectra taken right at the heterojunction are mixed with all three peaks being detected, indicating the presence of both materials around the actual interface. The spatial resolution of our confocal Raman microscope is near 1 μm. From the 2D Raman image we thus estimate the width of any intermixing between the two polymers in on a length scale less than 1 μm.

A schematic of the F8BT/TFB heterojunction LEFETs fabricated in bottom contact/top-gate configuration with PMMA dielectric and semitransparent gate electrode is shown in **Figure 5a**. The transfer characteristics, plotted in Figure 5b of these heterojunction LEFETs, have a more complex shape than those of pure F8BT LEFETs (compare Figure 5b and S9a with Figure 2b). For a gate voltage V_g less than about 40 V (with drain voltage V_d = 100 V) the device operates in unipolar hole mode. A hole accumulation layer is present in both the F8BT and TFB layers. Holes are injected from the TFB side across the relatively small energy barrier for holes at the heterointerface and are transported through the F8BT. For intermediate V_g between 40 and 80 V the current goes through a minimum and the device operates in the ambipolar regime. Here electrons are injected from the source contact into F8BT and holes injected from the drain contact into TFB and recombination occurs at a position inside the channel. However, for $V_g > 80$ V we do not enter into a unipolar electron regime as for pure F8BT LEFETs (Figure 2b), but the current decreases with increasing gate voltage instead. This is because TFB does not support the formation of an electron accumulation layer and electrons are unable to cross the large energy barrier between the LUMO levels of F8BT and TFB at the heterojunction.

During a transfer scan (with drain voltage V_d = 200 V) a well-defined, light-emitting recombination zone is observed to move along the channel (**Figure 6a**).[8] A corresponding video can be found in the Supporting Information. At around V_g = 70 V we begin to observe light emission from the edge of the electron injecting source electrode. Due to the relatively large F8BT electron mobility (0.5–1 × 10^{-3} cm^2 V^{-1} s^{-1}) compared to the TFB hole mobility (~10^{-4} cm^2 V^{-1} s^{-1}), the recombination zone moves rapidly throughout the F8BT region (V_g = 90 V)

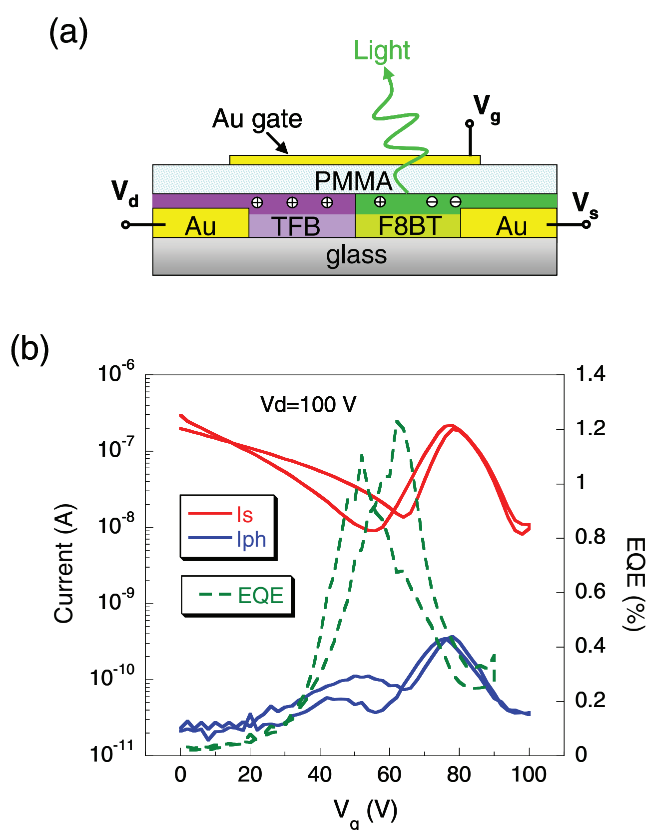

Figure 5. Device characteristics of F8BT/TFB heterojunction LEFET. a) Schematic illustration of a top-gate/bottom-contact LEFET with gold source/drain electrodes (20 nm thick), patterned F8BT/TFB (both about 40 nm thick) heterojunction in the middle of the channel, PMMA as the gate dielectric (~500 nm), and a semitransparent (10 nm) Au stripe as top-gate electrode. Also drawn are the electron and hole accumulation layers when the LEFET operates in the ambipolar regime, and radiative recombination occurs in the F8BT. b) Detected photocurrent (I_{ph}) and calculated EQE, deduced from the simultaneously recorded source current (I_s), of a heterojunction LEFET with L = 20 μm, W = 4000 μm at V_d = 100 V (V_s = 0 V) during a transfer scan with varying gate voltage V_g.

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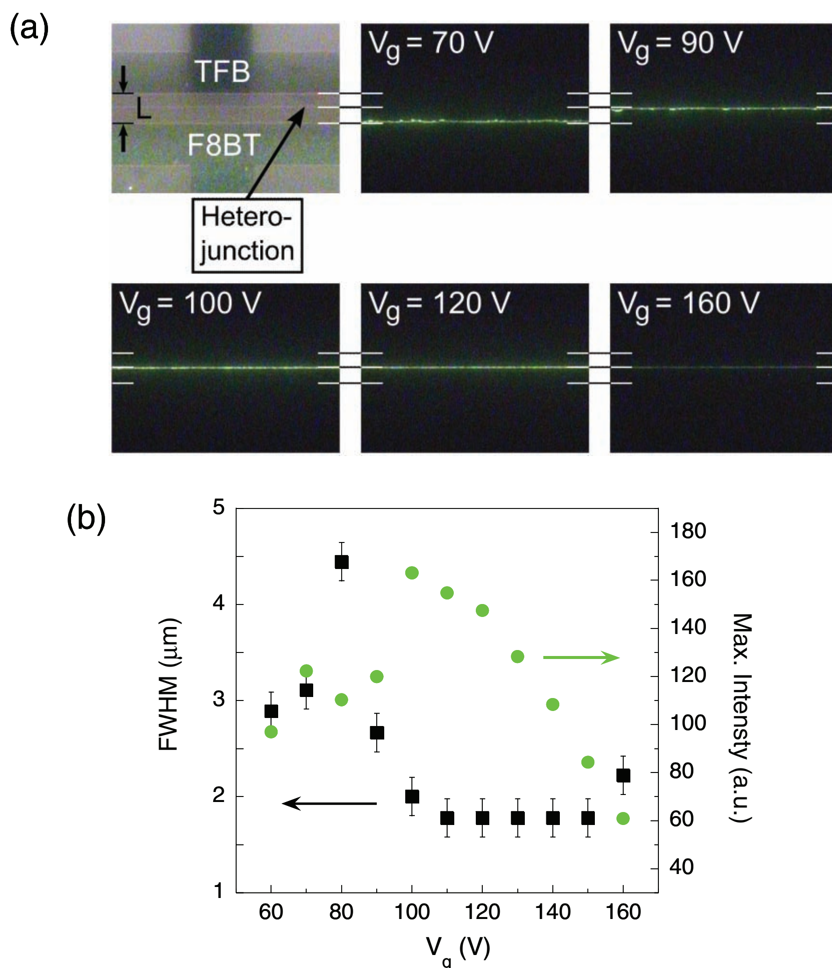

Figure 6. a) Digital camera snapshot images of the recombination zone moving within the transistor channel of length $L = 20$ µm during a transfer scan at $V_d = 200$ V and varied V_g. The relative position of the EL images taken under dark illumination conditions with respect to the source and drain electrodes and the heterojunction is indicated by white and black lines. The recombination zone starts off from the F8BT electrode at $V_g = 70$ V, reaches the heterojunction at $V_g = 100$ V and remains pinned at the heterojunction for higher V_g with steadily decreasing intensity. b) Extracted FWHM and maximum intensity of the converted light intensity of the recombination zone as a function of V_g.

into the vicinity of the heterojunction, and reaches it for $V_g \geq 100$ V. The light intensity is maximum at this point. When further increasing V_g the recombination zone remains pinned at the heterojunction and does not move into the TFB region. The light intensity drops steadily in this regime with increasing gate voltage as the TFB region becomes increasingly depleted of holes and the current drops. A summary of the dependence of the maximum intensity of the emitted light as a function of the gate voltage is shown in Figure 6b. At all voltages the electroluminescence (EL) spectrum (Figure S9c) is that of F8BT, even when the recombination zone is pinned directly at the heterojunction.

With a photodiode on top of the semitransparent gate electrode we have measured the photocurrent and extracted the external quantum efficiency (EQE) of the LEFET for light outcoupling through the semitransparent, thin gate electrode (Figure 5b; for a detailed calculation see the Supporting Information). The EQE during the transfer scan with $V_d = 100$ V is maximum when the recombination zone is starting to get pinned at the heterojunction around $V_g = 50$–70 V, which is the region of minimum current in the transfer scan. The maximum EQE is in the order of 1.2%. This is a high value and corresponds to near optimal internal quantum efficiency and complete recombination of electrons and holes.[34] Note that most of the emitted light is waveguided in the film/substrate and not detected here. The maximum EQE is higher by about 50% than that measured when the emission zone is located within the F8BT region (Figure 6b). This can be explained either by enhanced light outcoupling at the heterojunction or by the formation of intermediate exciplex states at the heterojunction, which could increase the singlet/triplet exciton ratio as a result of their small exchange energy.[29] In any case, the high EQE demonstrates the excellent quality of the heterojunction and excludes that luminescence-quenching sites are generated at the junction by the patterning process. This is particularly remarkable given that plasma etching and non-orthogonal solvents are used to define the side wall and the heterojunction, respectively.

Interestingly we observe a decrease in the full-width-at-half-maximum (FWHM) of the recombination zone from 3 µm when it is within the F8BT region to less than 2 µm when it becomes pinned at the heterojunction (Figure 6b). It is then limited by the optical resolution of our charge-coupled device (CCD) optical imaging system. This is a manifestation of the charge confinement at the heterojunction, and consequently an increased exciton density. Higher-resolution techniques such as scanning near-field optical microscopy (SNOM) will need to be used to resolve the true emission profile, but it is clear that by providing optical access to the interface the device architecture demonstrated here offers new opportunities for studying the recombination processes at such polymer heterojunctions.

The heterojunction LEFETs demonstrated here offer a number of important advantages compared to LEFETs based on a single ambipolar organic semiconductor. The recombination zone can be positioned robustly at a well-defined position in the channel, facilitating, for example, coupling of the emitted light into an integrated waveguide.[35] Such effective pinning of the light-emission zone has previously been demonstrated only in vertical diode-like devices with stacked semiconducting layers.[36] The structure allows separate optimization of electron and hole mobilities for the two materials adjacent at the heterojunction which should allow achieving higher current densities than those achievable with a single ambipolar semiconductor.[35,37–38] Heterojunction LEFETs are an attractive

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architecture for low-loss integrated optoelectronic devices and potentially electrically pumped lasing.

3. Conclusions

In conclusion, we have developed a simple, versatile, high-resolution patterning method for solution-processed organic semiconductors. Photolithographically patterned microstructures such as polymer ridges with a width of down to a micrometer have been realized. By employing a perfluorinated polymer such as Cytop as the protective layer for the underlying organic semiconductors throughout the lithography and plasma etching processes before its subsequent removal, no obvious degradation has been achieved in a variety of organic semiconductors for TFT applications. The unique properties of the perfluorinated polymer allow the patterning method to be compatible with all common transistor architectures. The significance of our photolithographic patterning process is therefore at least twofold. It provides a robust, broadly applicable technology for high-resolution patterning of polymer semiconductor active layer islands for applications in FETs, LEDs, and other devices without materials degradation, even when device performance depends critically on the quality of the top surface of the polymer film.

It also enables realization of novel heterojunction device architectures that have previously been difficult to fabricate with solution-processable organic semiconductors. Ambipolar light-emitting FETs based on lateral polymer/polymer heterojunctions with very little material degradation and high EL efficiency are a powerful example. Significant advantages of these heterojunction LEFETs compared to LEFETs based on a single ambipolar organic semiconductor are, for example, the possibility to fix the recombination zone at the heterojunction inside the channel and the charge carrier confinement at the heterojunction, which helps to achieve higher exciton densities and EQE. Moreover, it becomes possible to optimize electron and hole transport separately by selecting two appropriate organic semiconductors. As a result, higher current densities than in a single semiconductor ambipolar FET can be achieved, which is particularly important in the context of potential electrically pumped lasers. Our work therefore not only facilitates the material research based on device characterizations where precise confinement of current pathway is required, but also opens plenty of new possibilities to realize high-performance multi-polymer electronic devices for versatile optoelectronic applications.

4. Experimental Section

Materials: The polymeric semiconductors were obtained from the following suppliers: PBTTT (Mw = 28 kDa) from Prof. I. McCulloch and Prof. M. Heeney of Imperial College, London; P3HT (Mw = 22 kDa) from Merck Chemicals of United Kingdom; F8BT (Mw = 97 kDa) and TFB (Mw = 119 kDa) from Cambridge Display Technologies Ltd.; F8T2 (Mw = 60 kDa) from Sumation Co., Ltd.; P(NDI2OD-T2) (Mw = 250 kDa) from Polyera Corporation. PBTTT solutions were prepared in 1,2-dichlorobenzene (~8 mg mL^{-1}) and 1,2,4-trichlorobenzene (~5 mg mL^{-1}) for bottom-gate and top-gate FETs, respectively. P3HT solution was prepared in 1,2,4-trichlorobenzene with concentration of 10 mg mL^{-1}. Polymer solutions of F8BT, F8T2, and TFB were prepared in xylene with concentrations of 8, 7, and 10 mg mL^{-1}, respectively. P(NDI2OD-T2) solution was prepared in 1,2-dichlorobenzene with concentration of 9 mg mL^{-1}. The polymeric dielectrics were obtained from Cytop (product no. CTL-809M from Asahi Glass Co., see Figure S1a for chemical structure), PMMA (Mn = 255 kDa, from PolymerSource, Inc.). A fluorosolvent (perfluorotributylamine, product no. CT-Solv. 180 from Asahi Glass Co.) was used to dissolve Cytop. PMMA solutions were prepared in anhydrous *n*-butyl acetate (~45 mg mL^{-1}) to yield about 500 nm thickness. Polymeric semiconductors and dielectrics were deposited by spin-coating. All processing steps except photolithographic patterning were carried out in dry nitrogen.

Device Fabrication: All top-gate transistors, complementary inverters, and LEFETs were fabricated on Corning 1737F glass substrates. To realize top-gate organic FETs with shadow mask evaporated Al gate electrodes the organic semiconductor thin film to be patterned is spin-coated onto the substrate with predefined source/drain electrodes. Subsequently, a Cytop layer (~500 nm–1 μm) is spun on top (1, see Figure 1a). A thicker Cytop layer is typically found to facilitate the delamination, which is particularly useful in case of a lateral heterojunction. Due to its relatively low surface energy, it is very difficult to deposit photoresist (Shipley 1813) on top of the Cytop layer (2). Therefore, prior to photolithography it is required to make the Cytop surface hydrophilic. O_2 plasma treatment of the Cytop surface could cause serious damage to the semiconducting polymer/Cytop interface. Therefore, we opted instead to deposit a thin wetting layer of aluminum (1–2 nm). Such a thin aluminum layer can be etched within a few seconds in the developer of the photolithography process. By using a positive photoresist the regions where the polymer film is to remain on the substrate are protected by the photomask during the photolithography exposure (3). Hence, no UV-induced degradation can occur in these regions. Subsequently, the exposed photoresist and the thin aluminum layer underneath are removed using Shipley MF319 developer (4). During this processing step, which involves immersion into aqueous solutions, the underlying polymer is protected by the water-repelling Cytop. In the next step, the Cytop and the polymer film in the regions no longer covered by the photoresist are etched by O_2 plasma at 300 W for 10–20 min (5). After stripping the residual photoresist with acetone (6), the remaining Cytop film can be removed from the patterned semiconducting polymer surface by one of two methods (7): I) by using a fluorosolvent to dissolve Cytop, or II) by using adhesive tape (e.g., 3M Scotch tape) to delaminate the patterned Cytop and photoresist films. In the present work we delaminate the Cytop layer with an adhesive tape for all the patterned top-gate TFTs and heterojunction LEFETs.

Device Characterization: All FET characterizations were carried out in a dry nitrogen glove-box with an Agilent 4155B semiconductor parameter analyzer. For heterojunction LEFETs, light-emission intensities were measured with a silicon photodiode (Hamamatsu S1133-01) mounted directly above the transistor channel. EL spectra were recorded with an Ocean Optics HR4000 spectrometer using an optical multi-mode fiber. Optical images of the recombination zone were taken through the semitransparent gate electrode with a CCD color video camera and a 100 × objective.

Supporting Information

Supporting Information is available online from Wiley InterScience or from the authors.

Acknowledgements

J.-F. C. developed the patterning method, carried out the fabrication and characterization of the patterned films and devices. M. C. G. assisted in the fabrication and performed the measurements and analysis of the LEFETs. M. C. assisted in device preparation and measured inverter characteristics. T. S. assisted in development of the patterning approach.

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FULL PAPER

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